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TESIS DOCTORAL

The Power Recycling Distributed Amplifier

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Abstract

This Thesis introduces a novel distributed amplifier structure based on a power recycling scheme. This new architecture allows the amplifier gain to be enhanced while providing optimum output power and a perfect input match within a moderate bandwidth.

The ideal small signal performance of this novel distributed amplifier, called the power recycling distributed amplifier, has been analyzed based on the S-parameter matrix of an ideal and lossless directional coupler. The large signal performance of this novel amplifier has also been assessed. For this reason, a comprehensive analysis of the intrinsic power performance of distributed amplifiers, which is based on a simplified model of both the circuit and the active devices, has been carried out, emphasizing the role played by the dispersion diagram of the unit cells used. A complete discussion of the conditions leading to optimum designs, as far as the output power is concerned, is provided.

The Thesis highlights the advantages presented by the power recycling distributed amplifier compared to its counterparts in the field of distributed power amplification, along with its limitations, which are related to the mismatch and losses in the gate line.

Conclusions derived from the theoretical analysis have been validated through the design, manufacture and measure of two CRLH-TL-based distributed amplifiers, which demonstrate the viability of the power recycling distributed amplifier as an optimum class-A active power combiner with enhanced gain and excellent input match.

The work has been further extended with the evaluation of the proposed structure as a power amplifier working at high efficiency modes of operation. This evaluation concludes that this new architecture can also

work at various non-linear modes of operation, such as class AB, B or C, therefore increasing its efficiency, thanks to a proper selection of the bias conditions and a careful consideration of the load harmonics.

Resumen

La presente Tesis introduce una estructura novedosa de amplificador distribuido basada en un esquema que permite la reutilización de potencia. Esta nueva arquitectura permite incrementar la ganancia del amplificador proporcionando, al mismo tiempo, condiciones óptimas de potencia a la salida y de adaptación a la entrada para un ancho de banda moderado.

El funcionamiento en régimen de pequeña señal de este nuevo amplificador distribuido, conocido como amplificador distribuido en configuración *'power recycling'*, se ha analizado a partir de la matriz de parámetros S de un acoplador direccional ideal y sin pérdidas. Su funcionamiento en régimen de gran señal de dicho amplificador se ha evaluado también. Para ello, se ha realizado un analisis exhaustivo del comportamiento intrínseco en términos de potencia de los amplificadores distribuidos, basadao en un modelo simplificado tanto del circuito como de los dispositivos activos, en el cual se enfatiza el papel que desemplea el diagrama de dispersión de las celdas unitarias que componen el amplificador. Se ha incluido una completa discusión sobre las condiciones de fase que proporcionan condiciones de diseño óptimas, relativas a la potencia de salida.

La Tesis subraya las ventajas que presenta dicha configuración en comparación con sus homólogos en el campo de la amplificación de potencia distribuida, junto con sus limitaciones, que están relacionadas con la desadaptación y las pérdidas en la línea de puerta.

La conclusiones extraidas a partir del análisis teórico se han validado a través del disño, montaje y medida de dos prototipos de amplificador distribuido basados en líneas de transmisión CRLH. Lo cual demuestra

la viabilidad del amplificador distribuido *'power recycling'* como combinador óptimo de potencia en clase A con un incremento de ganancia y unos niveles de adaptación a la entrada excelentes.

El trabajo se ha extendido con la evaluación de la estructura propuesta como amplificador de potencia trabajando en clases más eficientes de operación. Dicha evaluación evidencia que esta nueva arquitectura puede trabajar en varios modos nolineales de operación, tales como la clase AB, B ó C, y por tanto incrementar su eficiencia, gracias a una correcta selección del punto de polarización y de las impedancias de los armónicos.

Contents

Chapter 1

Introduction

1.1 Contextual framework

Distributed amplification, first formulated by Percival in 1936 [1], was conceived as a means of combining the output power from several active devices. At the time, progress in the field of electronics called for an optimization both in the gain and in the bandwidth. Percival found that the gain-bandwidth product was greatly affected by the output capacitance of the active device and proposed a solution based on the absorption of these capacitances by artificial transmission lines. Percival's work was not fully appreciated until a decade later when Ginzton *et al.* [2] extended this concept. They pointed out most of the limitations of distributed amplification in terms of gain and bandwidth and several strategies to overcome them. Ginzton *et al.* also managed to create the first prototypes with good practical results [3]. Thereafter, distributed amplification has been used extensively to develop wideband amplifiers for a wide variety of applications [4; 5; 6; 7].

In contrast to the fast development of distributed amplification in small signal operation, it was not until 1984 when the distributed amplifier (DA) under large signal operation attracted a degree of attention. In this year Gamand *et al.* published a paper [8] in which they performed a distortion analysis to explain the DA behaviour under large signal operation. In that same year, Ayasli [9] presented an article in which he summarized the principles of distributed amplification and some experimental results. In this article, he devoted a section to power amplification

where he highlighted the power-limiting mechanisms of the classic architecture of the distributed amplifier. A significant drawback in this classic approach soon became apparent, that was related to its low efficiency. There are two key factors that cause it: the unequal power contribution of each active device and the power wasted in the idle port. The development of new standards in communications systems and the appearance of new, complex, digital waveforms gave rise to an evolution in the amplifiying stage. Therefore, distributed amplifiers were revisited over the years [10; 11; 12; 13; 14; 15; 16] in order to achieve a better performance in terms of efficiency and output power. However, in general, an increase in output power requires a sacrifice in the practical bandwidth, so a trade-off must be made.

The first attempts in literature sought an increase in both gain and output power by means of an output power combiner to recover the power lost in the idle port, and a simultaneous power injection in the input ports. This idea was presented by Aitchison *et al.* in 1988 [13], which was called dual-fed distributed amplifier, achieving gain improvements of up to 6dB in the overall gain of the structure. Although the performance of this architecture gave a significant improvement in gain and a reduction in noise figure at low frequencies, it soon was found that the structure was intrinsically mismatched. Moreover, the increasing development of RF applications required a bandpass behaviour rather than the lowpass exhibited by the structure. Along the same lines, Aitchison *et al.* published in 1989 a solution to the poor input match [17] by developing a balanced dual-fed amplifier. This solution combines two dual-fed circuits using two 90° hybrids. It presents, however, a very high circuital complexity, which is, probably, the reason for the lack of physical implementations of an architecture of this type. Meanwhile, in 1989 [18] Minnis developed a technique based on bandpass filter structures to achieve the desired bandpass behaviour to extend the frequency range, but from a small-signal point of view without considering the load conditions of the active devices.

In 1994 Campovecchio *et. al* [19] realized that to truly make the FET work in power operation, it was mandatory to pay attention to the load requirements of each active device. They proposed a method for optimum power matching which modifies the characteristic impedance and the electrical length of the stages in order to equalize the load impedances seen by the active devices. This strategy, on which the tapered drain lines [10; 11; 12] are based, however, does not exploit the power

delivered to the idle port. In some implementations, the idle port is terminated in an open circuit, reflecting a small portion of the power in the forward port, but at the expense of a deterioration in the output matching [11]. Practical implementations of this kind of amplifier have been measured demonstrating a good performance in terms of efficiency over a wide range, reporting a PAE of more than 27% over a 2-6 GHz bandwidth [12].

A similar approach is adopted by Narendra *et al.* in [20; 21], where the active devices are loaded with impedance termination values which are obtained from device load-pull measurements. These values can be designed by properly adjusting the current sources properties and the phase shifts between the stages. In [21], a PAE of more than 30% is obtained across a 10-1800 MHz frequency range.

The idea of the dual-fed distributed amplifier, which has already been proposed over the years [13; 14] and has achieved gain improvements of up to 6dB in the overall gain of the structure, was revived in 1999 by Eccleston *et al.* with a large signal perspective [22]. With this approach they tried to solve both issues, the use of the idle port and the unequal power contribution of the active devices. The load conditions for every single active device were analyzed, and it was demonstrated that if the proper electrical lengths and characteristic impedances are selected [15], it is possible to implement an optimum class-A power combiner. However, to physically implement it, Eccleston used a conventional transmission line to space the FETs by 180°, which resulted in rather large circuits. Furthermore, this alternative is inherently input mismatched, which is only mitigated by losses in the input line.

The introduction of the Composite Right/Left-Handed artificial transmission lines (CRLH-TLs), as an easy way of implementing 1D left-handed (LH) and right-handed (RH) propagation behaviours [23; 24; 25], opens up new opportunities in distributed power amplifier design. In fact, they are artificial TLs based on a particular (band-pass) unit cell topology. They offer a much richer frequency behaviour when compared with a conventional or RH-TL, thus leading to the development of novel microwave devices [23; 24].

Distributed circuits are based on propagation along artificial or continuous TL sections. Therefore they constitute an interesting field in which the innovation potential offered by CRLH-TLs can be tested. CRLH-TLs have already been used in distributed amplification and mixing to obtain new designs with novel functionalities

such as dual-band performance, diplexer functionality or image rejection (in the case of mixers) [26; 27; 28].

CRLH-TLs have demonstrated a great potential and versatility offering new applications to already known old problems. This feature, in itself, is reason enough to analyze what a metamaterial point of view may offer in distributed power amplification.

1.2 Motivation

The scenario described above provides insight into the motivation for this Thesis. Starting from the historical perspective of distributed power amplification, a question remains as to whether or not there is a solution that might satisfy the classic problems of this particular field, namely, the use of the idle port and the unequal power contribution of the active devices, without sacrificing the input match of the structure. At the same time, the fast spread of new applications based on metamaterials seems reason enough to examine the opportunities that this new structure might add to distributed power amplification.

In this context, the challenge ahead is to conduct a thorough study of the intrinsic behaviour of a generic distributed amplifier in terms of its loading conditions, so as to identify the design options for a Class A optimum power design. Following on from this idea, it seems appropriate to investigate whether the use of CRLH-TLs might add any interesting features to the work that has already been done up to date. In addition, new topologies will be sought that could provide a boost of the gain without a loss in the input match.

As in any other scientific work, experimental results will be sought that support the theory analysis. It is therefore a subject of this Thesis to design, manufacture and measure prototypes that might corroborate the aforementioned ideas.

The work would not be complete without further extending this study to more efficient modes of operations that can cope with the new complex modulation schemes. Although several works have been published related to this topic [29; 30], it would be of interest to cover the problem in a more comprehensive and structured way.

1.3 Thesis Outline

Chapter 2 is entirely devoted to the study of the intrinsic power and gain performance of a discrete distributed amplifier. This Chapter is a key part of being able to design a distributed power amplifier successfully. Starting from a generic scenario, the formulas that predict the load impedances at the intrinsic plane of the active devices are developed and thus their output power performance. From these formulas it is possible to determine the particular cases for which the amplifier works as an optimum class-A power combiner. Gain- and power-limiting aspects in distributed amplifier design are also considered.

Once the analysis of the intrinsic power and gain performance has been developed, the task of finding a solution that would deal with the classic problems of distributed power amplification arises. In ***Chapter 3***, a gain control mechanism is presented which provides perfect matching conditions at the input port. The idea is based on the work published by Nguyen *et al.* [31] and Wu *et al.* [32] for the maximization of the efficiency in leaky wave antennas. In this scheme the non-radiated power is fed back to the input port instead of being lost in the terminating load, the so-called power recycling concept. The same principle can be applied to distributed amplifiers. This configuration allows control over the gain level that can be, theoretically, as high as that desired, maintaining perfect matching conditions over a narrow operating band. The resulting distributed amplifier is called the Power Recycling Distributed Amplifier (PRDA).

Chapter 4 constitutes the proof of concept of previous Chapters. A prototype applying this design philosophy is presented in [16] with efficiency results close to the theoretical limit for Class A operation in a moderate bandwidth. The gain in the latter alternative can be improved by making some adjustments in the gate line. The application of a power splitter to introduce a simultaneous input power injection has already been proposed [13; 14], achieving gain improvements of up to 6dB in the overall gain of the structure. The downside of this alternative is an inherently input mismatch, which is only mitigated by losses in the input line. In a second version of the prototype, the input mismatch problem is solved by means of the proposed PRDA architecture. The experimental results demonstrate its viability as an optimum class-A active power combiner with enhanced gain and excellent

input match. The Chapter closes with a design in monolithic technology in order to address a more realistic challenge.

The work developed in previous Chapters is extended in ***Chapter 5*** with the study of the power recycling distributed amplifier working in high efficiency modes, which is a logical step in developing the PRDA's full potential as a power amplifier. The theory for the high efficiency amplifier modes will be reviewed and options in distributed power amplifier design will be addressed. A PRDA amplifier design in Class AB mode using high-power GaN HEMTs closes the Chapter.

Finally, ***Chapter 6*** summarizes the main results, and proposes future lines of action.

Chapter 2

Power and gain considerations in distributed amplifiers

2.1 Introduction

An analysis of the intrinsic power and gain performance of distributed amplifiers is described in this chapter. The analysis is based on a simplified model of both the circuit and the active devices (hence the so-called intrinsic performance) and emphasises the role played by the dispersion diagram of the unit cells used. A complete discussion of the conditions leading to optimum designs, as far as the output power is concerned, is provided. This analysis can be considered as an extension of that previously carried out by Eccleston [15]. A main result is that, by using CRLH unit cells, it is possible to design a distributed amplifier with an optimum output power performance and significant gain values [33], that can be further increased by means of the power recycling configuration (see chapter 3). The Chapter also includes the main power- and gain-limiting mechanisms that might degrade the performance of a distributed amplifier and several solutions proposed over the years to overcome them.

2.2 Intrinsic gain performance of distributed amplifiers

Distributed amplifiers are based on the active coupling of two TLs by periodically loading them with active devices. The generic topology of a uniform distributed amplifier can be easily inferred from Fig. 2.1. Notice that the artificial TLs are considered lossless and are terminated by their corresponding $Z_T(\omega)$ impedance, namely the image impedance of the unit cell with T-Topology [34].

The analysis of the intrinsic performance of distributed amplifiers is based on a unilateral, lossless and simplified model for the active device. Its equivalent circuit consists of a voltage-controlled current generator and two (input and output) capacitors (Fig. 2.2), which are absorbed into the shunt admitance of the unit-cells, which can be defined in T or π topology (see Appendix A.1).

A distributed amplifier is a four-port device, although usually just two of them are used as input and output ports, while the other two are loaded with the image or characteristic impedances of the corresponding unit-cells. Therefore it is possible to define two different gains in a distributed amplifier: forward (from port 1 to port 4 in Fig. 2.1) and reverse (from port 1 to port 3) gains.

The way a distributed amplifier works is pretty simple, the E_s input generator propagates a wave down the gate line with a phase shift of $\theta_g(\omega)$ per section, which excites the active device's input capacitances, C_{gsk}, producing a current in the drain line, $g_m V_{gsk}$, where the subscript k refers to any active device of the distributed amplifier. This wave will dissipate entirely in the right-hand load of the gate line. The current generated by each active device flows in both directions in the drain line with a phase shift of $\theta_d(\omega)$ per section. As a result, both output loads will dissipate power. This total amount of power dissipated by each output load can be easily computed by using the superposition principle. Each of the drain currents are obtained separately, and their contributions are summed up to calculate the total current in each output load.

The voltage at the input of the kth device is given by

$$V_{gsk} = V_{in} \cdot \sqrt{\frac{Z_{\pi g}(\omega)}{Z_{Tg}(\omega)}} \cdot e^{-j\left(\frac{2k-1}{2}\right)\theta_g(\omega)} \tag{2.1}$$

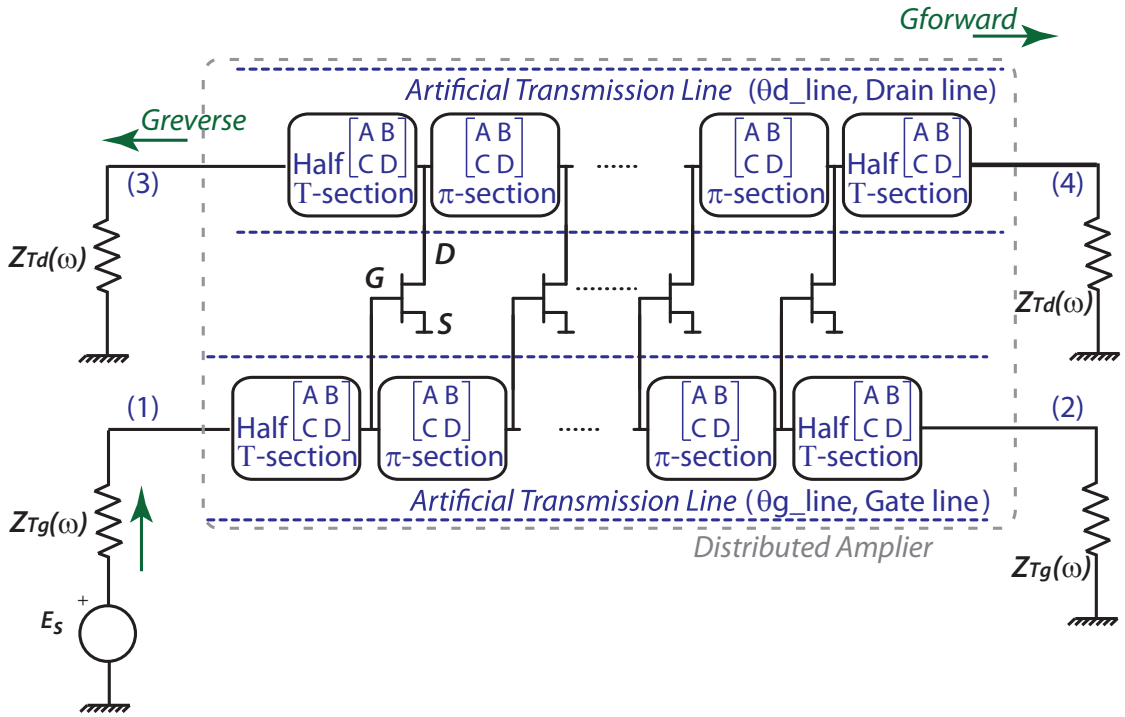


Figure 2.1: Generic distributed amplifier

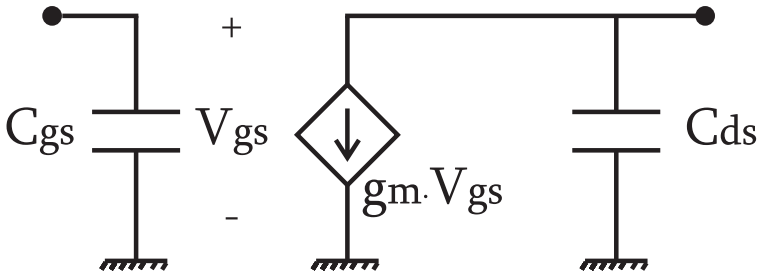


Figure 2.2: Simplified active device equivalent circuit

$Z_{\pi g}(\omega)$ being the image impedance with π-topology of the gate line. And the corresponding current components at the output is given by

$$I_{indk} = g_m \cdot V_{gsk} \tag{2.2}$$

From equations (2.1) and (2.2) it is easy to obtain the currents in the reverse and the forward port, where

$$Id_{forward} = \frac{1}{2}\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\{I_{ind1}\cdot e^{-j\theta_d(\omega)\frac{2n-1}{2}} + I_{ind2}\cdot e^{-j\theta_d(\omega)\frac{2n-3}{2}} + \cdots + I_{indn}\cdot e^{-j\frac{\theta_d(\omega)}{2}}\} \tag{2.3}$$

and

$$Id_{reverse} = \frac{1}{2}\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\{I_{ind1}\cdot e^{-j\theta_d(\omega)\frac{1}{2}} + I_{ind2}\cdot e^{-j\theta_d(\omega)\frac{3}{2}} + \cdots + I_{indn}\cdot e^{-j\theta_d(\omega)\frac{2n-1}{2}}\} \tag{2.4}$$

From these equations it is straightforward to calculate the power dissipated at the output ports as

$$Pdis_{forward} = \frac{1}{2}|Id_{forward}|^2\Re\{Z_{Td}(\omega)\} \tag{2.5}$$

$$Pdis_{reverse} = \frac{1}{2}|Id_{reverse}|^2\Re\{Z_{Td}(\omega)\} \tag{2.6}$$

and considering that the available input power is given by

$$Pav = \frac{|E_s|^2}{8\Re\{Z_{Tg}(\omega)\}} \tag{2.7}$$

it can be shown [34] that the available gains are given by

$$G_{forward} = \frac{g_m^2\Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}}{4}\frac{|Z_{\pi d}(\omega)||Z_{\pi g}(\omega)|}{|Z_{Td}(\omega)||Z_{Tg}(\omega)|}\left|\frac{\sin\left[\frac{N}{2}(\theta_d(\omega)-\theta_g(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_d(\omega)-\theta_g(\omega))\right]}\right|^2 \tag{2.8}$$

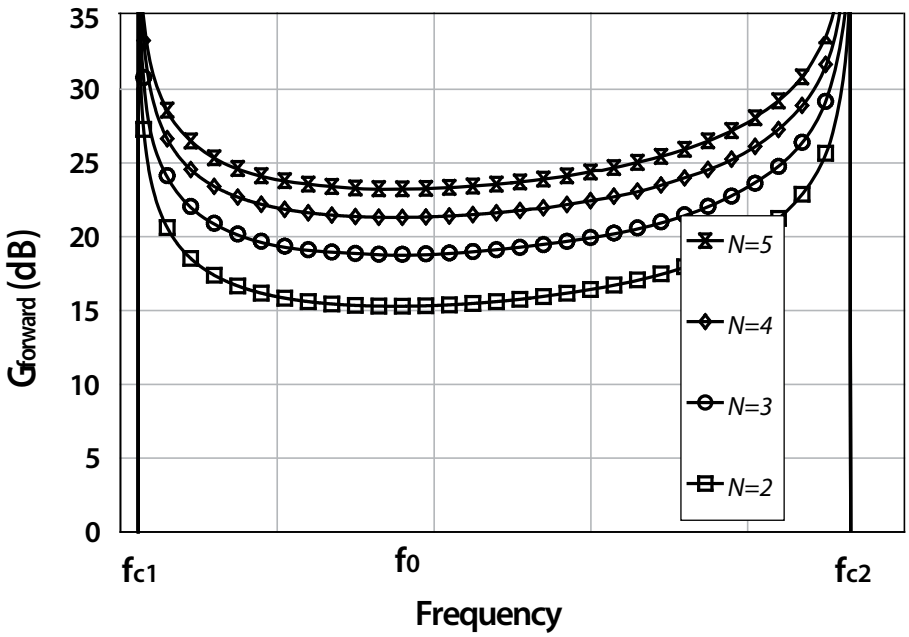


Figure 2.3: Forward gain of a CRLH-TL-based distributed amplifier for a different number of amplifier stages (f_{c1}, f_{c2} cutoff frequencies)

$$G_{reverse} = \frac{g_m^2 \Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}}{4} \frac{|Z_{\pi d}(\omega)||Z_{\pi g}(\omega)|}{|Z_{Td}(\omega)||Z_{Tg}(\omega)|} \left| \frac{\sin\left[\frac{N}{2}(\theta_d(\omega)+\theta_g(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_d(\omega)+\theta_g(\omega))\right]} \right|^2 \tag{2.9}$$

Equations (2.5-2.9) are only valid for the lossless case. It is worth noting that, apart from the frequency dependence associated with the image impedances of the unit cell with π-Topology of the gate and drain line, $Z_{\pi g}(\omega)$ and $Z_{\pi d}(\omega)$, the frequency behavior of both gains is controlled by the phase shifts, $\theta_g(\omega)$ and $\theta_d(\omega)$, of the unit cells, the transconductance, g_m, and the total number of active devices, N. It should also be noted that the forward gain is controlled by the difference in phase shifts, whereas the reverse gain depends on the sum of the phase shifts. In Figs. 2.3 and 2.4 the gain dependence with N and the load impedances with π-topology is depicted for the particular case of a band-pass distributed amplifier ($\theta_g(\omega) = \theta_d(\omega)\,\forall\,\omega$

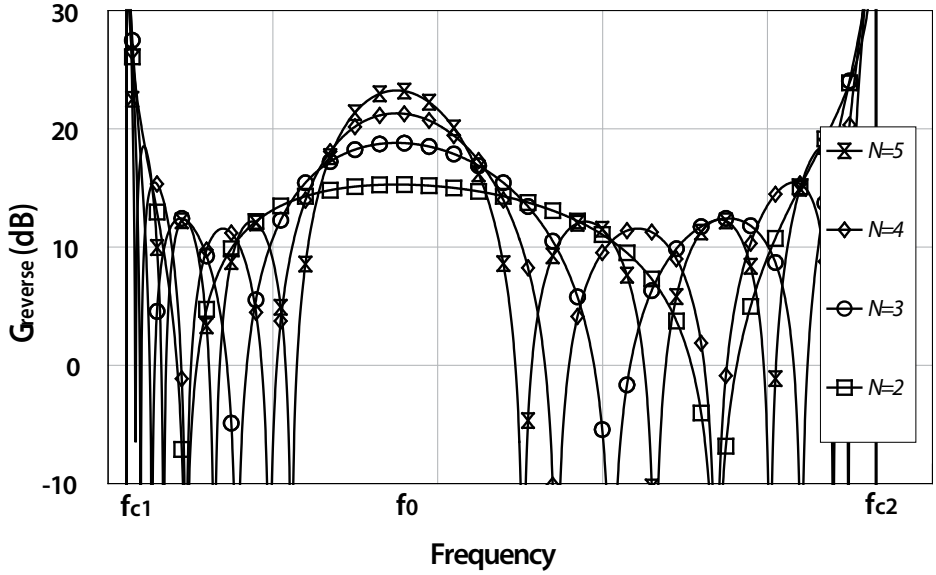


Figure 2.4: Reverse gain of a CRLH-TL-based distributed amplifier for a different number of amplifier stages

and a CRLH dispersion diagram) (See section A.2). The dependence on frequency of the image impedance with π-Topology is the reason for the gain regrowth near the cut-off frequencies. In subsection 2.5 some strategies proposed over the years to equalize the frequency response are described. The relationship with the number of active devices can be easily inferred from equations 2.8 and 2.9. If the following conditions are fulfilled: $\theta_d(\omega) - \theta_g(\omega) = 0 \pm 2m\pi$ and $\theta_d(\omega) + \theta_g(\omega) = 0 \pm 2m\pi$, m being an integer (m=0,1,2,..), then the following approximations can be assumed:

$$\left| \frac{\sin\left[\frac{N}{2}(\theta_d(\omega) - \theta_g(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_d(\omega) - \theta_g(\omega))\right]} \right| \rightarrow N \tag{2.10}$$

and

$$\left| \frac{\sin\left[\frac{N}{2}(\theta_d(\omega) + \theta_g(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_d(\omega) + \theta_g(\omega))\right]} \right| \rightarrow N \tag{2.11}$$

Since the $\theta_g = \theta_d$ condition has been selected for the gain simulation, dependence with N^2 is exhibited for the forward gain in the whole frequency range as seen in

Fig. 2.3. However, this conclusion is only true for the reverse gain (see Fig. 2.4) for a frequency range near f_0 and next to the cut-off frequencies. Therefore, it can be concluded that the forward gain presents a wideband behaviour that can be made as large as that desired by means of increasing the number of stages, while the reverse gain exhibit a maximum value just for certain frequency points.

This approach is the one that is normally used in a conventional distributed amplifier design. Low-pass (or RH TLs) unit cells are used and the condition $\theta_g(\omega) = \theta_d(\omega)$ is imposed, which results in a wideband behavior (limited by the cut-off frequencies of the unit cells) for the forward gain and in a low-pass behavior with a limited bandwidth for the reverse gain. This results in a maximum value for the forward gain in a frequency range only limited by the cut-off frequencies of the unit cells and in a maximum value for the reverse gain at $f = 0$. This is why only ports 1 and 4 are used when broadband amplification is the design aim. However, novel design choices emerge if other unit cells, with a richer frequency behavior than that provided by band-pass or CRLH unit cells (see A.2) are considered [28].

The first remarkable feature of using CRLH-TLs instead of the conventional RH TLs is the transformation in the frequency response from a low-pass behaviour to a band-pass one (see Fig. 2.5 versus Fig. 2.6). This might be useful when working at higher frequency ranges. Some previous works have been published in the subject [18; 35].

The second interesting feature is to explore different design options for the dispersion diagrams in the gate and the drain line. By using different slopes in the drain and the gate lines it is possible to achieve a maximum in the gain response at different, designable, frequency points, which can be exploited to achieve a diplexer functionality (Fig. 2.7).

Finally, by using a richer dispersion diagram it is possible to recover the power that it is traditionally wasted in the idle port in a conventional RH-TL-based distributed amplifier. If both dispersion diagrams are selected to present, for instance, the $\theta = 0$ for the same operation frequency f_0, both the forward and the reverse gain exhibit maximum gain conditions (Fig. 2.6).

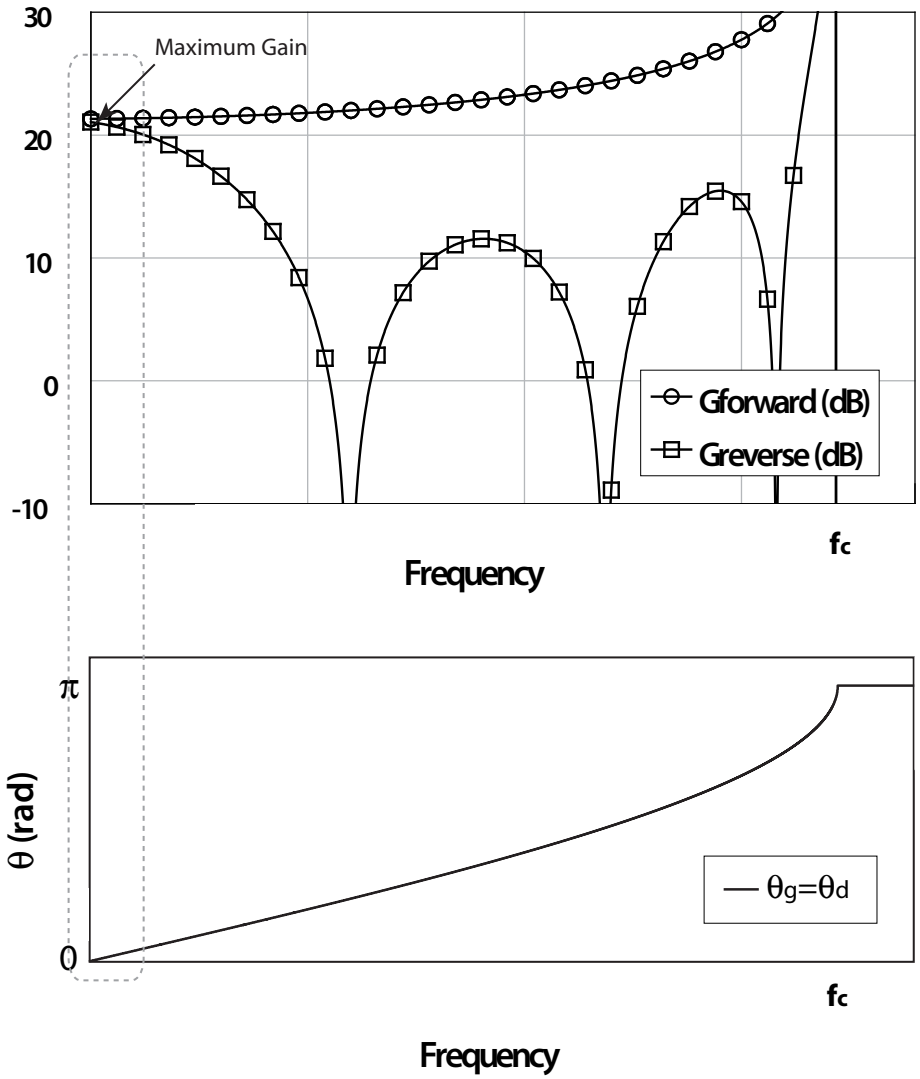


Figure 2.5: Forward and reverse gain of a 4-stage RH-TL-based distributed amplifier with identical gate and drain phase constants

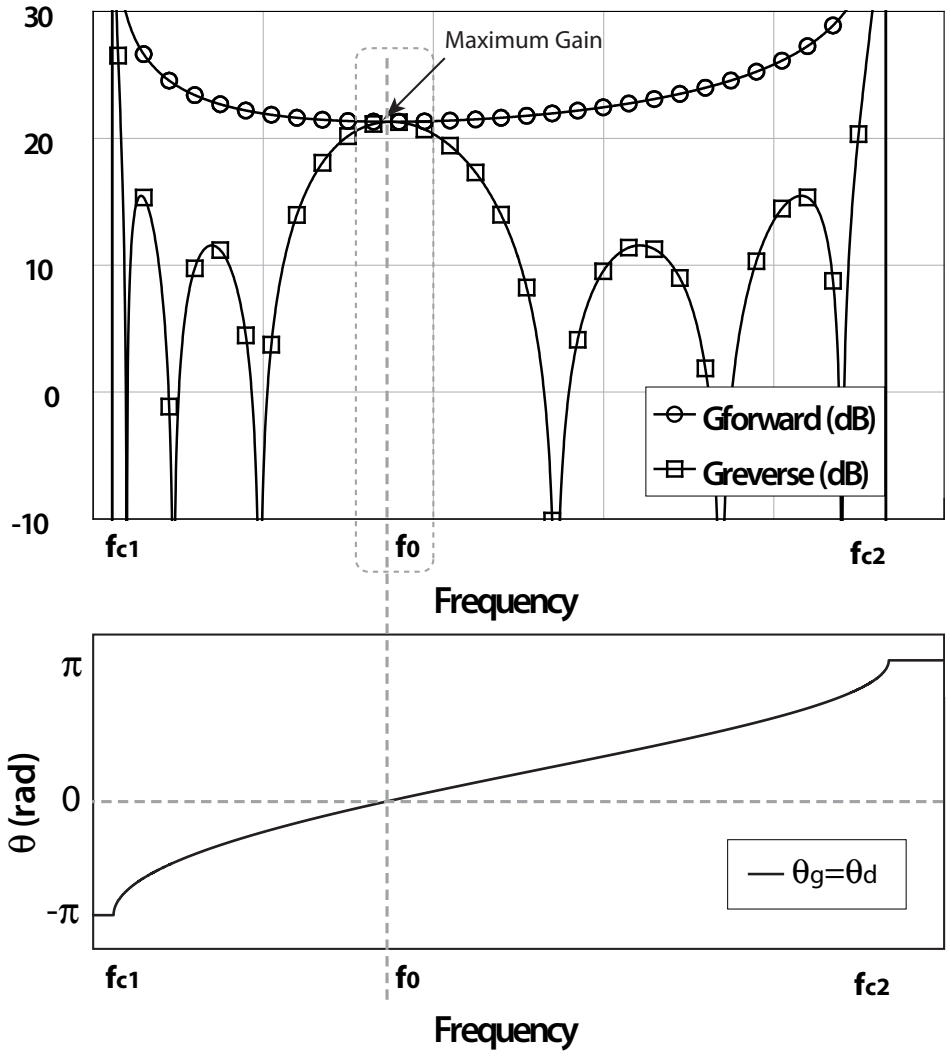


Figure 2.6: Forward and reverse gain of a 4-stage CRLH-TL-based distributed amplifier with identical gate and drain phase constants

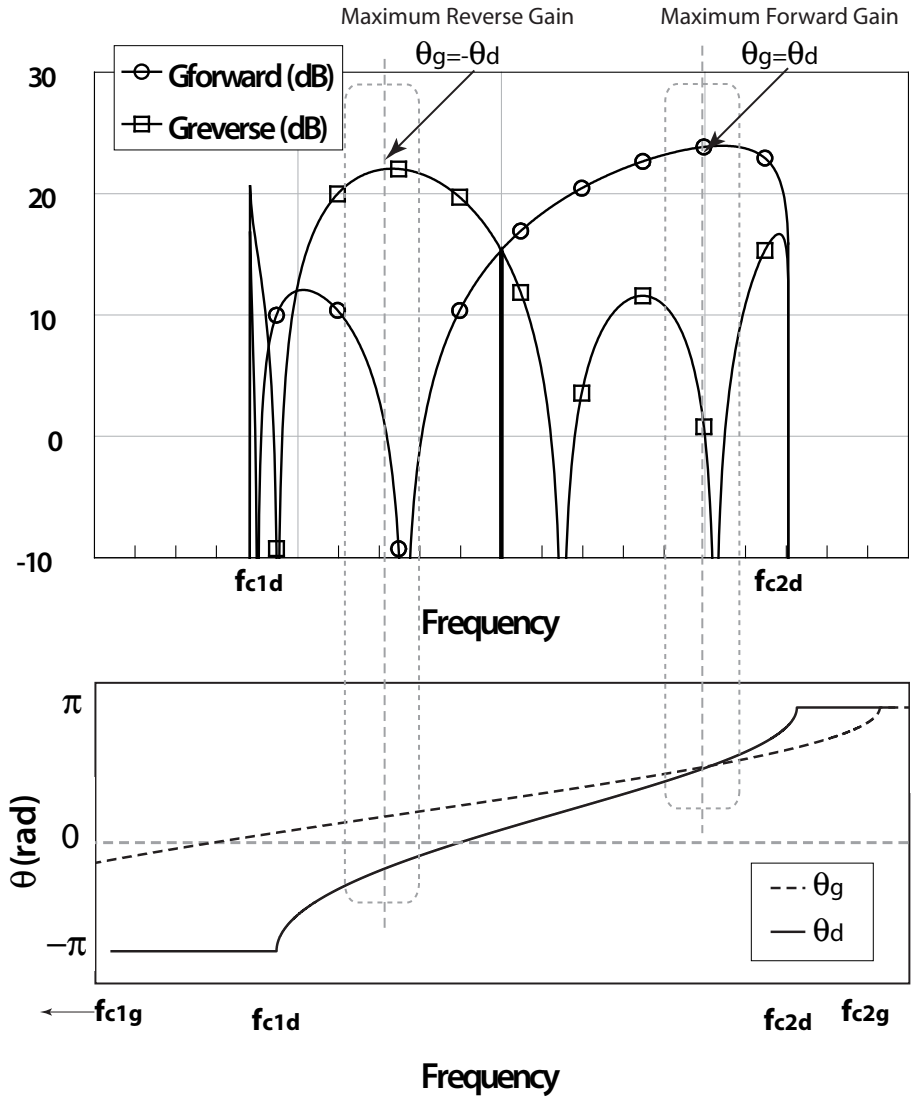


Figure 2.7: Forward and reverse gain of a 4-stage CRLH-TL-based distributed amplifier with different gate and drain phase constants

2.3 Power considerations

The generalised distributed amplifier detailed in Fig. 2.1 can also be used to assess its intrinsic power performance. Under the simplifying assumptions introduced both in the distributed amplifier structure and in the active device equivalent circuit, the power delivered by each active device is controlled by the load impedance at its reference plane. Therefore these load impedances (Z_{Lk}) are the key point in the discussion of the intrinsic power performance of distributed amplifiers.

Using the superposition principle, the voltage at the output intrinsic plane of the kth device can be easily computed, resulting in

$$V_k = \sum_{l=1}^{N} V_k^l = Z_{\pi d}(\omega)\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\sum_{l=1}^{N}\frac{I_{indl}}{2}e^{-j\theta_d(\omega)|k-l|} \tag{2.12}$$

Taking into account that the load impedance, Z_{Lk}, at the intrinsic plane of the kth device is defined by

$$Z_{Lk}(\omega) = \frac{V_k}{I_{indk}} \tag{2.13}$$

the following equations can be obtained:

- If $k \leq \frac{N}{2}$, N-even or $k \leq \frac{N+1}{2}$, N-odd

$$\begin{aligned} Z_{Lk}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\Bigg[& e^{j(\theta_g(\omega)-\theta_d(\omega))\frac{k}{2}}\frac{\sin\left[\frac{(k-1)}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]} \\ & + e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(N-k)}{2}}\frac{\sin\left[\frac{(N+1-k)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\Bigg] \end{aligned} \tag{2.14}$$

- If $k > \frac{N}{2}$, N-even or $k > \frac{N+1}{2}$, N-odd

$$Z_{Lk}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\left[e^{-j(\theta_g(\omega)-\theta_d(\omega))\frac{(1-k)}{2}}\frac{\sin\left[\frac{k}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}\right. \\ \left. + e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(N-k+1)}{2}}\frac{\sin\left[\frac{(N-k)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\right] \tag{2.15}$$

These two equations show that, in general, the load impedance of each active device at a given frequency is different and therefore they contribute with different power levels to the power delivered by the distributed amplifier. The maximum output power requires the load impedance for each device to be real and equal to its optimum value (Fig. 2.8). This optimum value is given by (class-A) [36]

$$R_{Lopt} = V_{dc}/(I_{max}/2) = V_{dc}/I_{dc} \tag{2.16}$$

provided that the device is biased at the quiescent point defined by

$$I_{dc} = \frac{I_{max}}{2}, V_{dc} = \frac{V_{max}}{2} \tag{2.17}$$

Also, from equations (2.14) and (2.15) it can be easily shown that the load impedance Z_{Lk} takes a real value given by

$$Z_{Lk} = \frac{N}{2}Z_{\pi d}\sqrt{\frac{Z_{\pi d}}{Z_{Td}}} \tag{2.18}$$

when $\theta_g = \theta_d = \pm m\pi$ or when $\theta_g = -\theta_d = \pm m\pi$, m being an integer (m=0,1,2,...). Eq. 2.18 can be reduced to:

$$Z_{Lk} = \frac{N}{2}Z_{\pi d} \tag{2.19}$$

for the particular phase shift values in which $Z_{\pi d} = Z_{Td}$.

This means that, under any of these conditions, each device contributes, with the same power level, to the amplifier output power. If the unit cell is designed, according to (2.19), so as to provide the optimum real load impedance required by the device, the maximum amplifier output power is achieved. These results agree

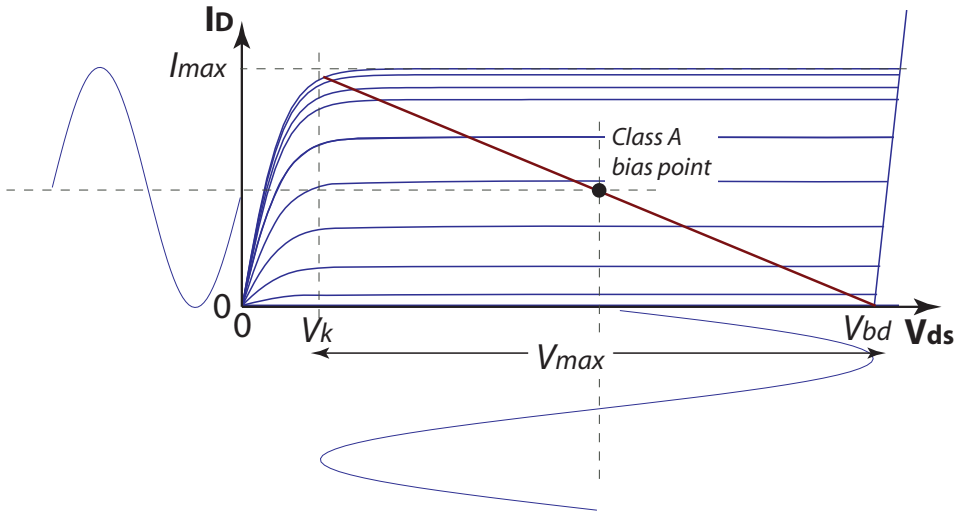


Figure 2.8: Optimum Class A load line for maximum voltage and current excursion

with those previously obtained by Eccleston [15].

As an illustrative example, let us consider a five-stage distributed amplifier. The normalised power (with respect to its maximum value) delivered by the third device as a function of gate and drain phase shifts is detailed in Fig. 2.9. Optimum choices for θ_g and θ_d clearly arise from this figure. Note that both the negative and positive values of the phase shifts have been considered since both of them can be provided by the CRLH unit cells. Zero values are of particular interest since they can be implemented at any arbitrary frequency by using CRLH (band-pass) unit cells. Their use was proposed by Eccleston [37] to shorten the length of the resulting distributed amplifier as well as increase the bandwidth.

The influence of gate and drain phase shifts on forward and reverse gains has been represented in Figs. 2.10 and 2.11, respectively, for the 5-stage distributed amplifier. It is clear from these figures that maximum values will be obtained when $\theta_g(\omega) = \theta_d(\omega)$ for the forward gain and when $\theta_g(\omega) = -\theta_d(\omega)$ for the reverse gain. This means that through the proper design of the gate and drain phase shifts it is possible to obtain maximum output power from each active device and maximum values for both gains (forward and reverse) at a given frequency.

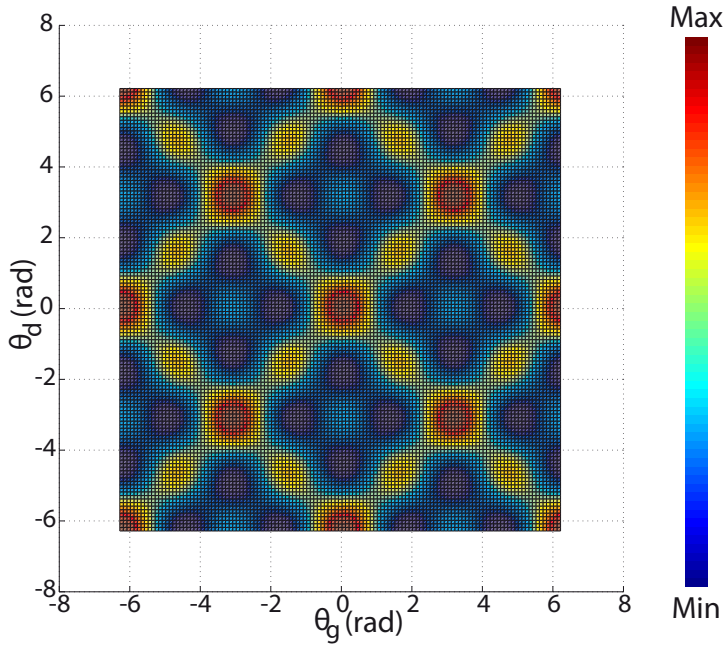


Figure 2.9: Normalized power delivered by the 3^{rd}-stage of a 5-stage distributed amplifier as a function of gate and drain phase shifts (red areas represent maximum power values)

2.4 Dual-fed configuration

The power and gain performance of distributed amplifiers can be further improved by using both gate ports to inject the input signal (Fig. 2.12). This configuration is called 'dual-fed' and was first proposed by Aitchison *et al.* [13]. The basic idea is to take advantage of the four existing gain paths when the signal is injected through both input ports to increase the gain and of the two output ports to extract all the available output power.

The analysis described in Section 2.3 showed that it is possible to design a distributed amplifier to exhibit the maximum of its four gains at a given frequency. Splitting the input signal and combining the two output ports provide a 6 dB increase in the overall gain of the amplifier when compared with the single-fed configuration.

Moreover, the combination of the two output signals eliminates the output power wastage in the reverse port and provides a 3 dB increase in the output power.

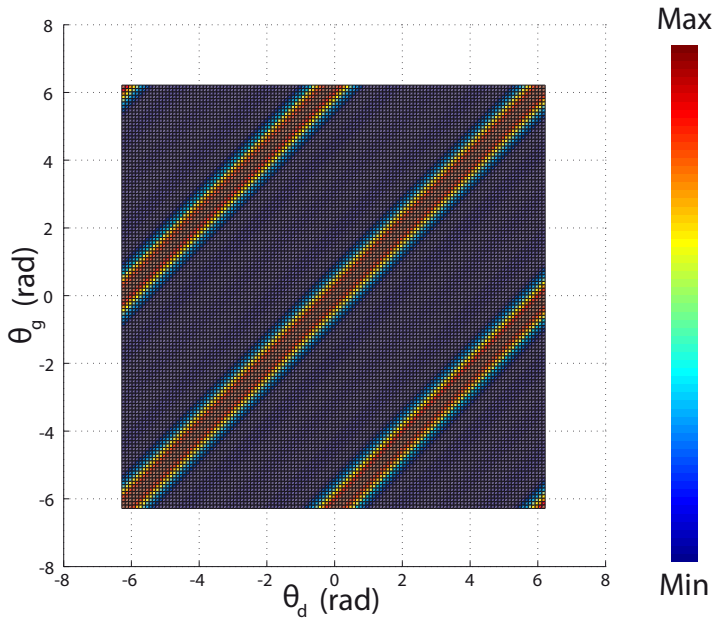


Figure 2.10: Output power at the forward port for a 5-stage single-fed distributed amplifier as a function of gate and drain phase shifts (red areas represent maximum power values)

However, the previously obtained expressions for the load impedance (2.14-2.15) are not valid when a signal is injected simultaneously through both input ports.

2.4.1 Power performance of the dual-fed distributed amplifier

By using the same analysis methodology as that presented in Section 2.3, alternative expressions for the load impedances can be obtained in a straightforward manner. The simultaneous input signal injection makes it necessary to apply twice the superposition principle. The voltage at the output ports is computed considering that excitation only exists at a single input port. Therefore, two different solutions are achieved (one solution for each input voltage generator), that will be sum afterwards. The voltage at the input of the kth device is given by

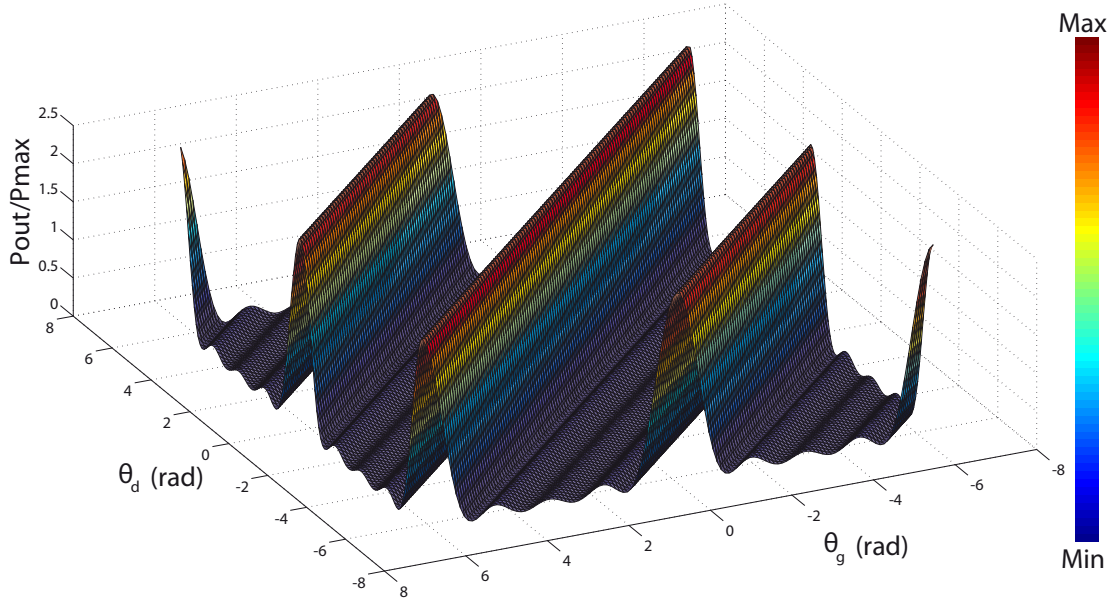


Figure 2.11: Output power at the reverse port for a 5-stage single-fed distributed amplifier as a function of gate and drain phase shifts (red areas represent maximum power values)

$$V_{gk}(\omega) = V_{in} e^{-j\frac{1}{2}\theta_g(\omega)} \left[e^{-j(k-1)\theta_g(\omega)} + e^{-j(n-k)\theta_g(\omega)} e^{j\phi} \right] \sqrt{\frac{Z_{\pi g}(\omega)}{Z_{Tg}(\omega)}} \tag{2.20}$$

and the corresponding current components at the output by (2.2). Using the superposition principle, the voltage at the output intrinsic plane of the kth device can be computed, resulting in

$$V_k(\omega) = V_k^{(1)}(\omega) + V_k^{(2)}(\omega) \tag{2.21}$$

where the (1) and (2) superscripts are related with the active input signal generator, and being $V_k^{(1)}(\omega)$ and $V_k^{(2)}(\omega)$

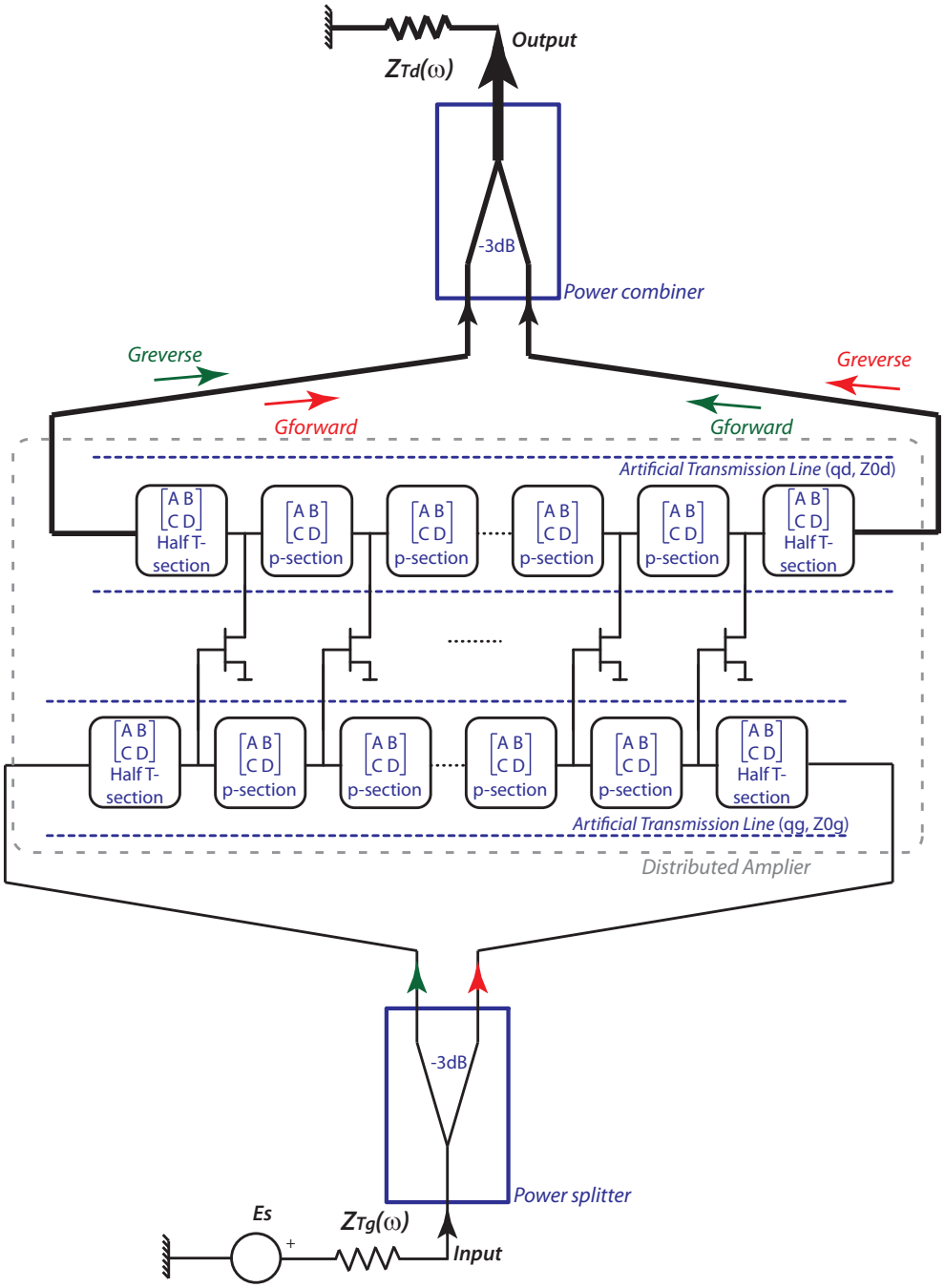


Figure 2.12: Generic dual-fed distributed amplifier

- If $k \leq \frac{N}{2}$, N-even or $k \leq \frac{N+1}{2}$, N-odd

$$V_k^{(1)}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)Z_{\pi g}(\omega)}{Z_{Td}(\omega)Z_{Tg}(\omega)}}g_m e^{-j\left(\frac{2k-1}{2}\right)\theta_g(\omega)}V_{in} \cdot \left[e^{j(\theta_g(\omega)-\theta_d(\omega))\frac{k}{2}}\frac{\sin\left[\frac{(k-1)}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}\right] + \left[e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(n-k)}{2}}\frac{\sin\left[\frac{(n+1-k)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\right] \tag{2.22}$$

$$V_k^{(2)}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)Z_{\pi g}(\omega)}{Z_{Td}(\omega)Z_{Tg}(\omega)}}g_m e^{-j\left(n-k+\frac{1}{2}\right)\theta_g(\omega)}V_{in}e^{j\phi} \cdot \left[e^{-j(\theta_g(\omega)-\theta_d(\omega))\frac{(k-n)}{2}}\frac{\sin\left[\frac{(n+1-k)}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}\right] + \left[e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(k)}{2}}\frac{\sin\left[\frac{(k-1)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\right] \tag{2.23}$$

- If $k > \frac{N}{2}$, N-even or $k > \frac{N+1}{2}$, N-odd

$$V_k^{(1)}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)Z_{\pi g}(\omega)}{Z_{Td}(\omega)Z_{Tg}(\omega)}}g_m e^{-j\left(\frac{2k-1}{2}\right)\theta_g}V_{in} \cdot \left[e^{-j(\theta_g(\omega)-\theta_d(\omega))\frac{(1-k)}{2}}\frac{\sin\left[\frac{k}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}\right] + \left[e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(n-k+1)}{2}}\frac{\sin\left[\frac{(n-k)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\right] \tag{2.24}$$

$$V_k^{(2)}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)Z_{\pi g}(\omega)}{Z_{Td}(\omega)Z_{Tg}(\omega)}}g_m e^{-j\left(n-k+\frac{1}{2}\right)\theta_g(\omega)}V_{in}e^{j\phi} \cdot \left[e^{j(\theta_g(\omega)-\theta_d(\omega))\frac{(n+1-k)}{2}}\frac{\sin\left[\frac{(n-k)}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}\right] + \left[e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(k-1)}{2}}\frac{\sin\left[\frac{k}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\right] \tag{2.25}$$

where ϕ is the phase difference between the input voltages. The load impedance can be computed as the ratio between (2.21) and (2.2).

Different cases of simultaneous injection can be considered. The same load impedance for each active device can be achieved in the dual-fed case if $\theta_g = \theta_d$ or $\theta_g = -\theta_d$, and if any of the following conditions is fulfilled:

(a) $\theta_g = \pm 2m\pi$ (in-phase input voltages – $\phi = 0$)

(b) $\theta_g = \pm(2m+1)\pi$ (anti-phase input voltages – $\phi = \pi$, N-even)

(c) $\theta_g = \pm(2m+1)\pi$ (in-phase input voltages – $\phi = 0$, N-odd)

In all cases, the load impedance are the same as before, that is, $Z_{Lk} = \frac{N}{2}Z_{\pi d}\sqrt{\frac{Z_{\pi d}}{Z_{Td}}}$. Conclusions extracted from this analysis are, basically, the same as those mentioned for the single-fed distributed amplifier. The analysis shows that if a proper selection of the phase shifts between stages is made for the gate and the drain line it is possible to achieve the same load impedance for each active device. In those particular cases, this value happens to be real, which allows a dual-fed distributed amplifier to be designed where each active device will deliver its maximum available output power working in a class-A mode of operation.

2.4.2 Gain performance of the dual-fed distributed amplifier

To analyze the gain performance of a dual-fed distributed amplifier Fig. 2.12 will be studied. It shows a generic dual-fed distributed amplifier, where the artificial transmission lines have been plotted as a discrete set of 2-port networks, represented

by their corresponding $ABCD$-matrixes. Its small-signal response is easily achievable by applying the superposition principle both in the input and the output lines of the circuit. The circuital schematic on Fig. 2.13 is proposed for the analysis. The input power has been split equally between the two input ports of the structure. ϕ is the phase shift between the two signals. If just one input signal generator is active at the time it is easy to compute the output by following the same approach as in section 2.2 . By adding the current contributions to the output ports delivered by each one of the input ports, the total output current after the power combination, I_{output}, can be computed, as can any other figure of merit such as the gain or the output power.

The qualitative behaviour of the dual-fed distributed amplifier can be easily explained through equation (2.20). When simultaneous power injection is applied the voltage at the input of the active devices is computed as the addition of both signal contributions. If the phase conditions for maximum output power described in section 2.4.1 are fulfilled it is evident that $|V_{gsk}| = 2|V_{in}|$, where $V_{in} = \frac{E_s}{2\sqrt{2}}$, therefore, the addition of both input signals is constructive. Furthermore, under such circumstances, the phase of the input voltages of the N active devices is the same. A generic expression for the gain can be obtained applying equations (2.2-2.4) and (2.20). For the optimum phase shifts conditions described in the previous subsection, the expressions for the current, the gain and output power are as follows:

$$I_{forward\ dual-fed} = I_{reverse\ dual-fed} = \frac{E_s}{2\sqrt{2}} N g_m \sqrt{\frac{Z_{\pi d}(\omega) Z_{\pi g}(\omega)}{Z_{Td}(\omega) Z_{Tg}(\omega)}} \tag{2.26}$$

$$P_{forward\ dual-fed} = P_{reverse\ dual-fed} = \frac{|E_s|^2}{8} N^2 g_m^2 \left| \frac{Z_{\pi d}(\omega) Z_{\pi g}(\omega)}{Z_{Td}(\omega) Z_{Tg}(\omega)} \right| \Re\{Z_{Td}(\omega)\} \tag{2.27}$$

$$P_{output\ dual-fed} = P_{forward\ dual-fed} + P_{reverse\ dual-fed} \tag{2.28}$$

$$P_{av} = \frac{|E_s|^2}{4\Re\{Z_{Tg}(\omega)\}} \tag{2.29}$$

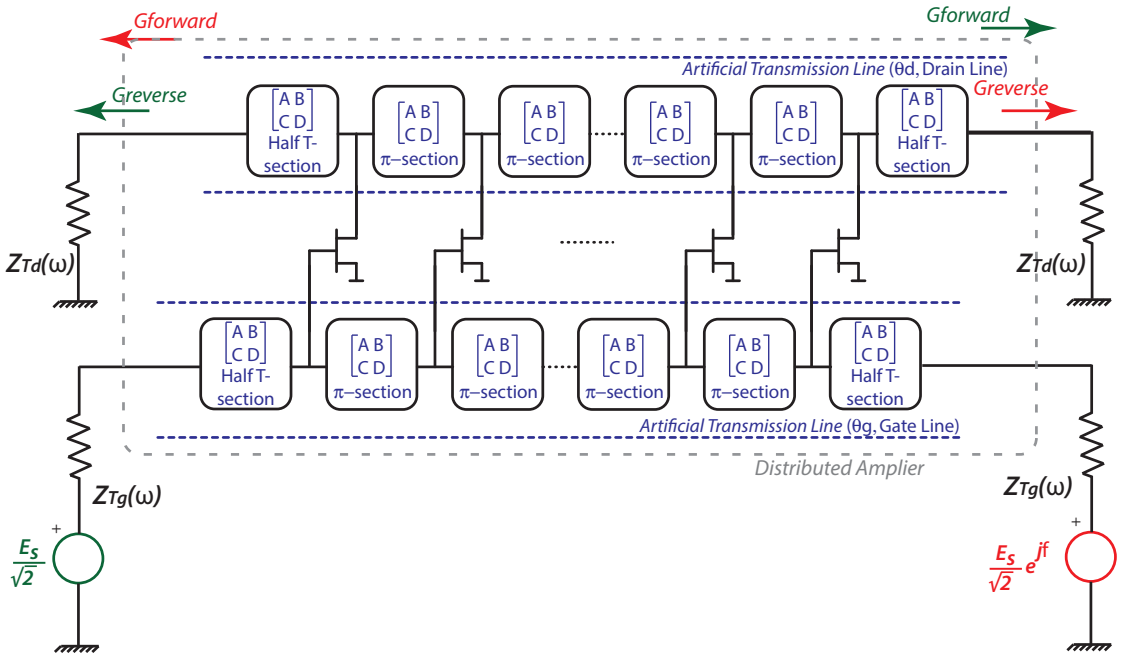


Figure 2.13: Generic dual-fed distributed amplifier equivalent circuit

$$G_{dual-fed} = \frac{P_{output\ dual-fed}}{P_{av}} = N^2 g_m^2 \Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}\left|\frac{Z_{\pi d}(\omega)Z_{\pi g}(\omega)}{Z_{Td}(\omega)Z_{Tg}(\omega)}\right| \quad (2.30)$$

2.5 Power- and gain-limiting mechanisms

Equations 2.8 and 2.9 indicates that the gain can be increased without limit, maintaining a constant bandwidth, by increasing the total number of active devices, N. However, this only applies in an ideal lossless case. In fact, there are several limiting mechanisms that must be taken into account when facing a real implementation [9]. In this section, the most important mechanisms will be reviewed.

2.5.1 Gain-limiting mechanisms

Losses in the gate and drain line. In practice, the gain does not increase monotonically with N because of losses in the gate and drain lines. The addition

of active devices can increase the total output power, but requires an increase in the length in the gate and the drain lines. A point will be reached when the loss of power in the added drain line section cannot be overtaken by the power introduced by a new active device. To evaluate this effect, the attenuation constant, α, must be introduced in the propagation constant. Considering this, the equations for the forward and reverse gain can now be obtained, where:

$$G_{forward} = \frac{g_m^2 \Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}|e^{-N(\gamma_g(\omega)+\gamma_d(\omega))}|}{4} \cdot \frac{|Z_{\pi d}(\omega)||Z_{\pi g}(\omega)|}{|Z_{Td}(\omega)||Z_{Tg}(\omega)|} \left| \frac{\sinh\left[\frac{N}{2}(\gamma_d(\omega)-\gamma_g(\omega))\right]}{\sinh\left[\frac{1}{2}(\gamma_d(\omega)-\gamma_g(\omega))\right]} \right|^2 \tag{2.31}$$

$$G_{reverse} = \frac{g_m^2 \Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}|e^{-N(\gamma_g(\omega)+\gamma_d(\omega))}|}{4} \cdot \frac{|Z_{\pi d}(\omega)||Z_{\pi g}(\omega)|}{|Z_{Td}(\omega)||Z_{Tg}(\omega)|} \left| \frac{\sinh\left[\frac{N}{2}(\gamma_d(\omega)+\gamma_g(\omega))\right]}{\sinh\left[\frac{1}{2}(\gamma_d(\omega)+\gamma_g(\omega))\right]} \right|^2 \tag{2.32}$$

In Figs. 2.14 and 2.15 the simulation of the forward and reverse gains for a different number of amplifier stages is shown with a constant attenuation per section of 1.5 dB in both artificial transmission lines. A point is reached where any further increase in the total number of active devices will result in a reduction in the total output power. The optimum number of active devices can be easily computed by maximizing the gain expression with respect to N [34; 38].

Capacitive drain-gate coupling. The analysis based on unilateral models of active devices is not valid if the input-output isolation is not very high. To include this feature, a more complete model for the active device is mandatory, such as the one shown in Fig. 2.16 . The formulation, with the inclusion of the coupling between the gate and the drain ports, may not lead to close-form solutions, so numerical methods will have to be used. In practice, CAD software tools offer a direct solution to resolve the system equations.

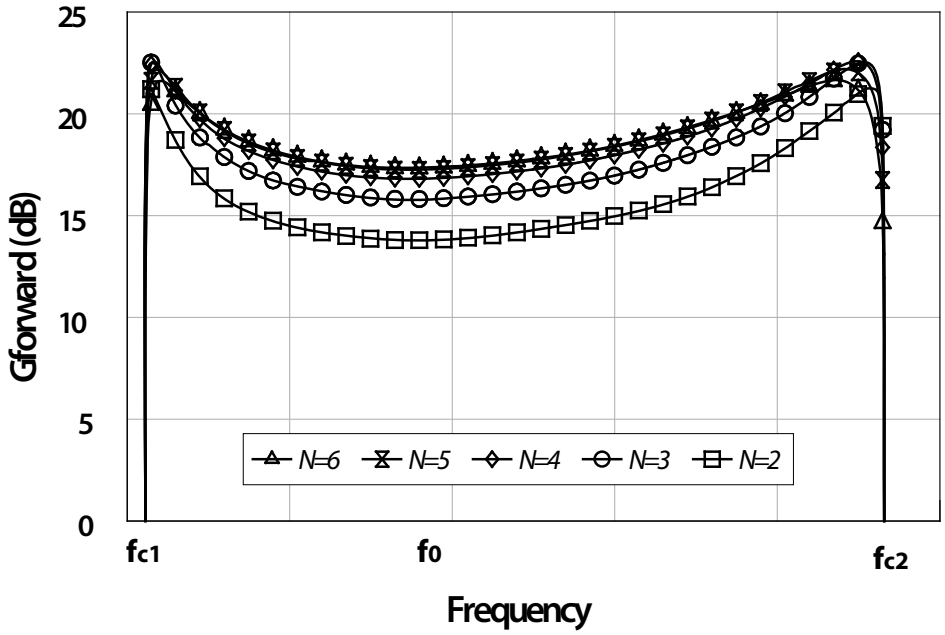


Figure 2.14: Effect of losses ($\alpha = 1.5dB$ per stage) on the forward gain of a CRLH-TL-based distributed amplifier as a number of amplifier stages

Mismatch at the end of gate and drain lines. Impedance variation with frequency impose restrictions on the performance of distributed amplifiers. The power and gain analysis detailed in the previous sections is based in the image impedance theory. The influence of this impedance, $Z_{i\pi}(\omega)$, produce a voltage increase near the cutoff frequencies. This behaviour is straightforward from Fig. 2.3. Although, in practice, such an impedance cannot be synthesized, the gain performance of distributed amplifiers still presents such a voltage increase (see Fig. 2.19). Several strategies has been proposed over the years to improve the amplifier performance:

- In 1948, the use of artificial transmission lines made up of m-derived sections was proposed by Ginzton et al. [2]. By using the m-derived section (Fig. 2.17) there will still be the problem of a non-constant image impedance, but a new degree of freedom is introduced, m, which can be chosen to minimize the variation of $Z_{i\pi}(\omega)$ over the passband of the filter [34; 39].

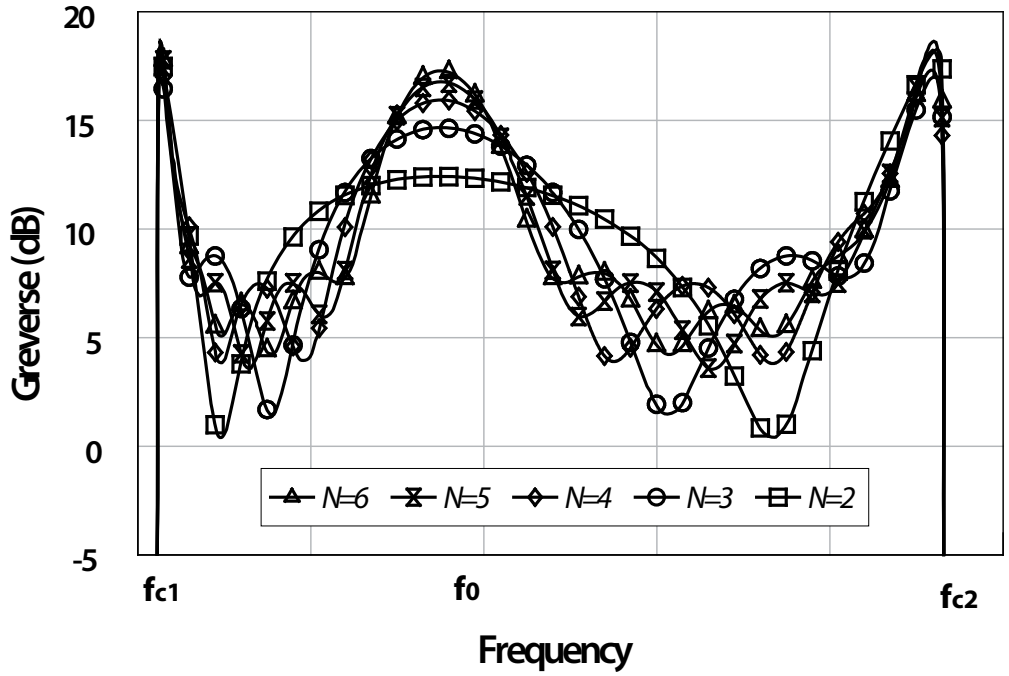


Figure 2.15: Effect of losses ($\alpha = 1.5dB$ per stage) on the reverse gain of a CRLH-TL-based distributed amplifier as a number of amplifier stages

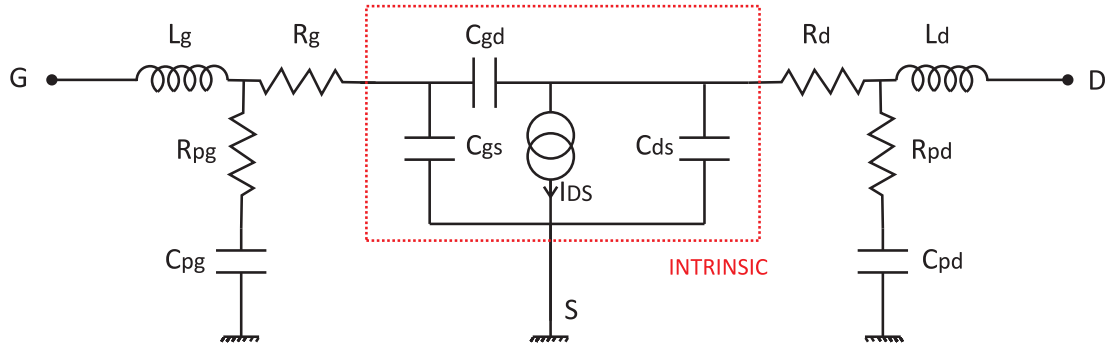


Figure 2.16: Small-signal equivalent circuit for a GaN active device

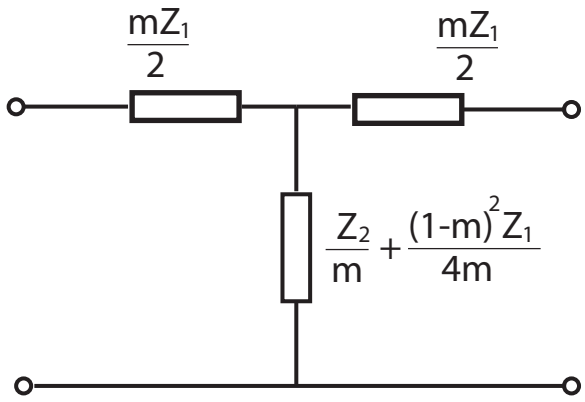


Figure 2.17: m-derived section with T-topology

- The use of bridged-T sections is another alternative, first proposed by Ginzton et al. (1948) to suppress the impedance variation with frequency. The equivalent circuit of a bridged-T section is presented in Fig. 2.18, and it can be demonstrated that, if properly designed, it becomes an all-pass network with a constant characteristic impedance.

- Designing the input and output lines to present different cutoff frequencies can result in an improvement in gain and delay uniformity.

2.5.2 Power-limiting mechanisms

There are four main power-limiting mechanisms related to distributed amplifiers.

Finite RF voltage swing that can be allowed in the input gate line The forward conduction and the pinch-off voltage of the device limit the the RF voltage swing in the positive and negative RF cycle, respectively. For a class A mode of operation, the maximum input RF power to the amplifier is given by

$$P_{in,max} = \frac{(Forward\,voltage - Pinchoff\,voltage)^2}{8\Re\{Z_g\}} \tag{2.33}$$

The maximum output power will be given by $P_{in,max} \times G$.

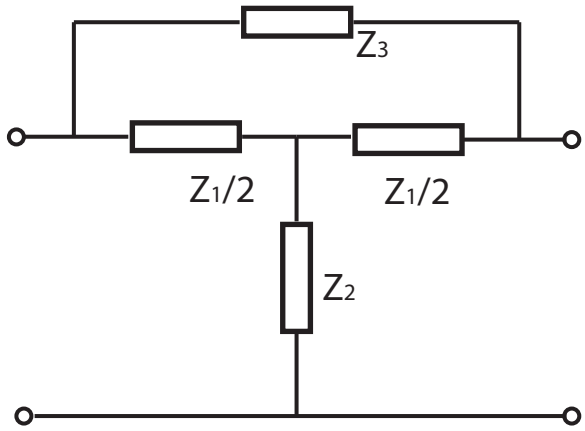


Figure 2.18: Bridged-T section

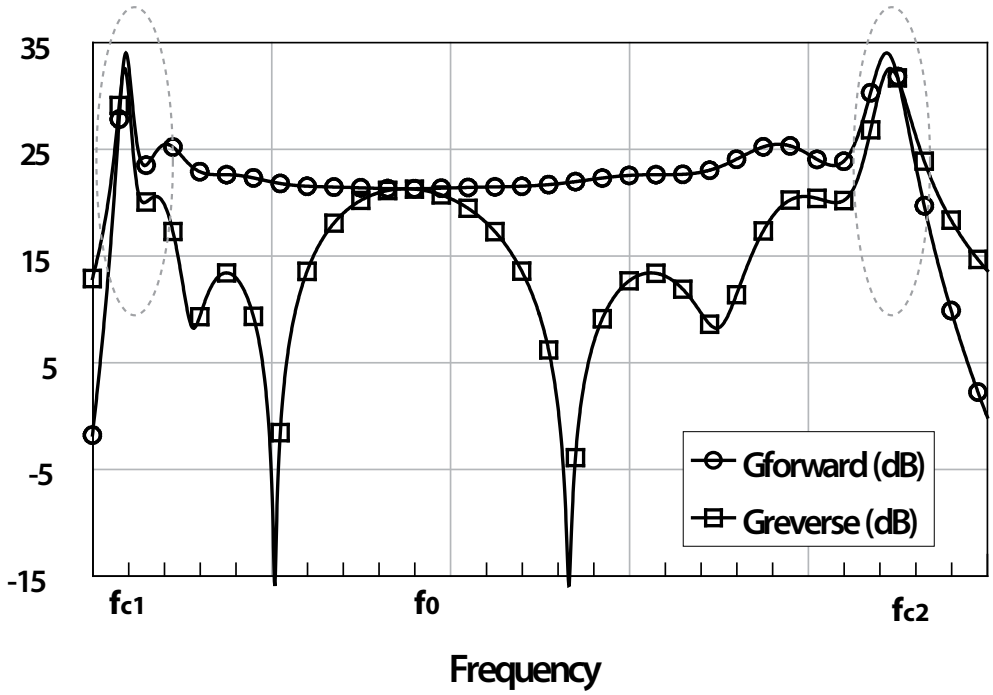


Figure 2.19: Forward and reverse gain of a 4-stage CRLH-TL-based distributed amplifier with identical phase constants terminated with an 50Ω load impedance

Maximum total gate periphery for a single-stage design. The output power capabilities of the active device can be increased with a larger gate periphery, however, it will also affect to the gate line attenuation. A limit in the total gate periphery is set to maximize the gain and, therefore, the maximum output power.

Optimum RF load requirements. Given a certain periphery of the FET unit, the optimum RF load impedance is fixed. This value will establish the characteristic drain line impedance if the number of stages, N, is set (see equation 2.19).

Gate-drain breakdown voltage of the FETs The drain terminals must support the RF swing of the amplified output signal.

2.6 Summary

This first Chapter summarizes the already-known theory for the design of distributed amplifiers in the small signal regime. The analysis is extended to a more general case which covers different kind of dispersion diagrams for the artificial transmission lines (eg. CRLH-TLs).

The Chapter also discusses the behaviour of the structure as a power amplifier by calculating the load impedance of each active device at the operation frequency. Closed-form expressions for the load impedance were obtained and used to discuss the influence of the phase shifts of the unit cells on the intrinsic power performance. The results obtained suggest that the use of CRLH or band-pass unit cells provides the designer with new choices which can be used, for instance, to optimise the output power performance of distributed amplifiers.

The Chapter finally presents the main power and gain limiting mechanisms that can be encountered when facing a physical implementation along with several solutions and considerations proposed over the years to overcome them.

Chapter 3

The Power Recycling Distributed Amplifier

3.1 Introduction

In this Chapter a novel distributed amplifier structure based on a power recycling scheme is proposed. It allows the amplifier gain to be enhanced while providing optimum output power and a perfect input match within a moderate bandwidth. The ideal performance of this novel distributed amplifier, called the power recycling distributed amplifier (PRDA), is analyzed. The structure overcomes the problems presented by the dual-fed configuration. Limitations introduced by mismatch and losses in the gate line have also been assessed.

3.2 Theory of operation

Any distributed amplifier can be understood as the active coupling of two transmission lines by periodically loading them with active devices (Fig. 2.1). The gate line feeds the active device inputs whilst the drain line combines the amplified output signals. If proper phase shifts for gate and drain unit cells are chosen, broadband amplifier performance can be achieved [2] but at the price of reduced power efficiency since the active devices do not contribute equally to the output power. To ensure that all the devices provide the same power it is necessary for all the load

lines at their intrinsic reference planes to be identical. Moreover, if these load lines are designed to be the device optimum for class-A operation, the resulting amplifier can be considered as an optimum power combiner since it could ideally add the maximum power supplied by an arbitrary number of active devices. This condition can only be fulfilled at a discrete set of gate and drain unit-cells phase shifts (see Section 2.3).

Under such conditions the intrinsic load impedance is the same for all devices and takes the value given by equation (2.19). Moreover, the output power delivered at the forward and reverse output ports of the distributed amplifier are exactly the same. Thus, a power combiner at the output ports allows the maximum power to be extracted that can be delivered by the active devices under class-A operation. If a single-fed topology is chosen, ideally a perfect input match is achieved although the gain value is limited by the constraint imposed by equation (2.19). If, on the other hand, a dual-fed topology is used, a 6 dB increase in the gain is obtained but at the price of worsening the input match (ideally, a complete mismatch). Nevertheless, this concept has been recently validated experimentally using CRLH unit-cells to reduce the circuit size [16]. The PRDA proposed in this chapter combines the power maximization provided by the proper design of the unit-cell phase shifts and the gain enhancement provided by the use of a power recycling scheme [31; 32] in the gate transmission line. The basic architecture of a PRDA is detailed in Fig. 3.1. It is based on a distributed amplifier designed for power maximization. A combiner collects the forward and reverse output ports, while the gate line is fed back thanks to a directional coupler (symmetrical or antisymmetrical) and two additional transmission line sections (Z_0, θ_{aux1} and θ_{aux2}).

Basically, the input power injected into port 6 will be partly directed towards port 5, therefore into the distributed amplifier's gate transmission line, and partly to the matched port (port 8). The injection of this power wave, b_5, into the gate line will generate the a_7 wave, that will be re-injected into the hybrid ring. Again, part of this energy will end up in the matched port, whilst the remaining fraction will contribute to the increase in the b_5 wave providing a proper phase shift is selected for the auxiliary line.

Through a proper design, this novel distributed amplifier can provide maximum output power and, at the same time, a perfect input match as well as gain control

or enhancement.

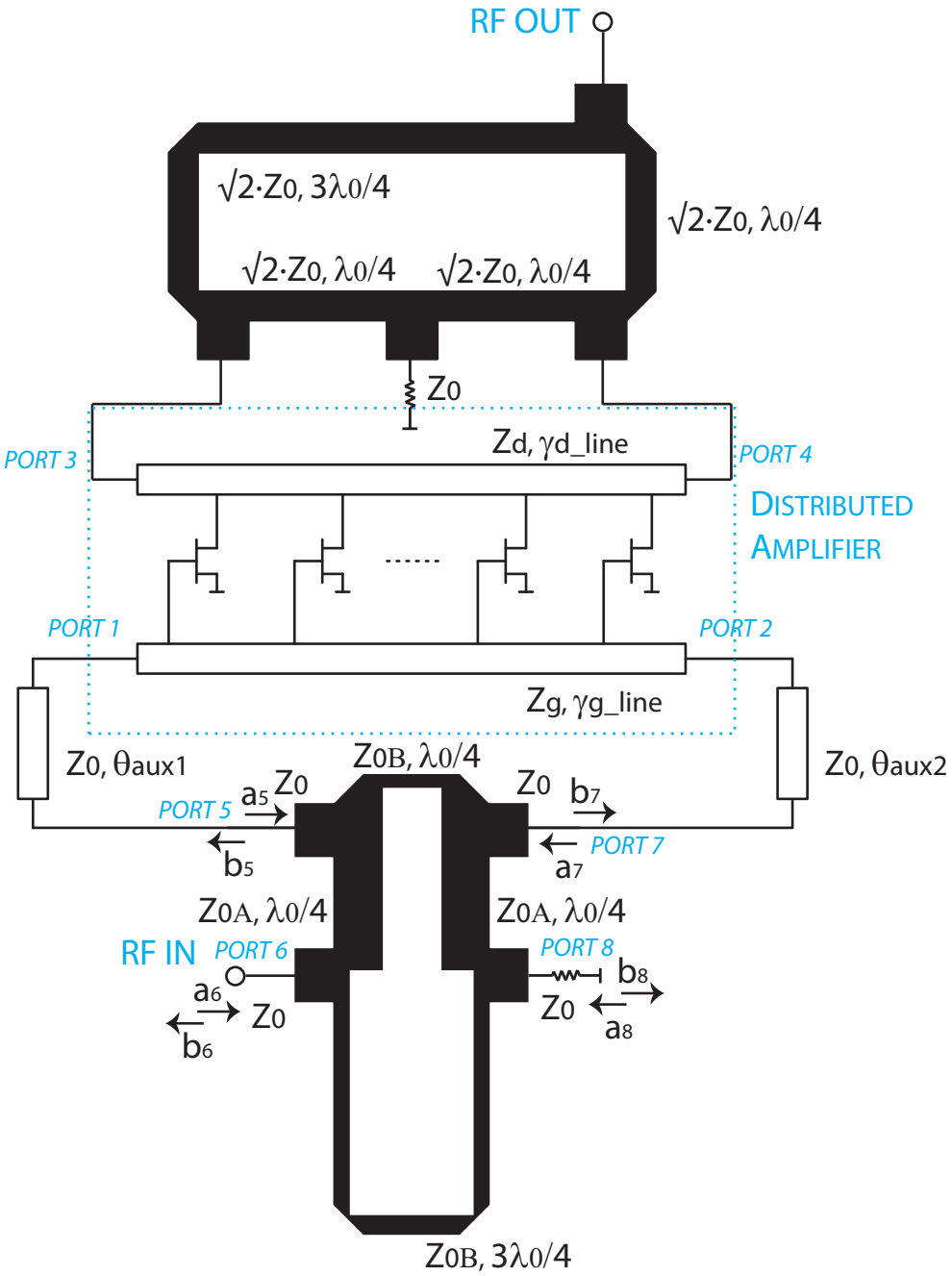


Figure 3.1: 180°-based implementation of the power recycling distributed amplifier

3.2.1 Intrinsic performance

To discuss the intrinsic performance, i.e. the best performance that can be achieved under ideal conditions, a simplified analysis is carried out. The analysis relies on the idea proposed by Nguyen *et. al* [31] for the maximization of the efficiency of leaky wave antennas. For the sake of completeness, results published in [31] will be partially reproduced in this section. The distributed amplifier is considered to be unilateral and the gate line is modeled by a lossless transmission line of characteristic impedance Z_0 and electrical length θ_{g_line}. The additional transmission lines also have Z_0 and are lossless (θ_{aux1} and θ_{aux2}). The directional coupler is also ideal and lossless with an antisymmetrical response (the symmetrical response will be also discussed later on). Under these simplifying assumptions, and taking into account that the S-parameter matrix of an ideal and lossless antisymmetrical directional coupler is given by [39]

$$[S] = -j \begin{bmatrix} 0 & A & B & 0 \\ A & 0 & 0 & -B \\ B & 0 & 0 & A \\ 0 & -B & A & 0 \end{bmatrix}, A^2 + B^2 = 1; A, B \in \mathbb{R} \tag{3.1}$$

It is straightforward to obtain the value for the power wave entering port 5, namely [40]

$$b_5 = \frac{-jA \cdot a_6}{1 + jB \cdot e^{-j(\theta_{g\_line} + \theta_{aux1} + \theta_{aux2})}} \tag{3.2}$$

and also, that $a_5 = b_6 = b_7 = 0$. $b_8 = 0$ means that the structure exhibits a perfect match, while $a_5 = b_7 = 0$ indicates that there is only one wave propagating along the gate line from port 5 to port 7. Therefore, the overall gain of the amplifier is governed by the ratio b_5/a_6. Equation (3.2) clearly indicates that this ratio is, for a given value of the coupling, maximum if [31]

$$e^{-j(\theta_{g\_line} + \theta_{aux1} + \theta_{aux2})} = j \tag{3.3}$$

that is [40],

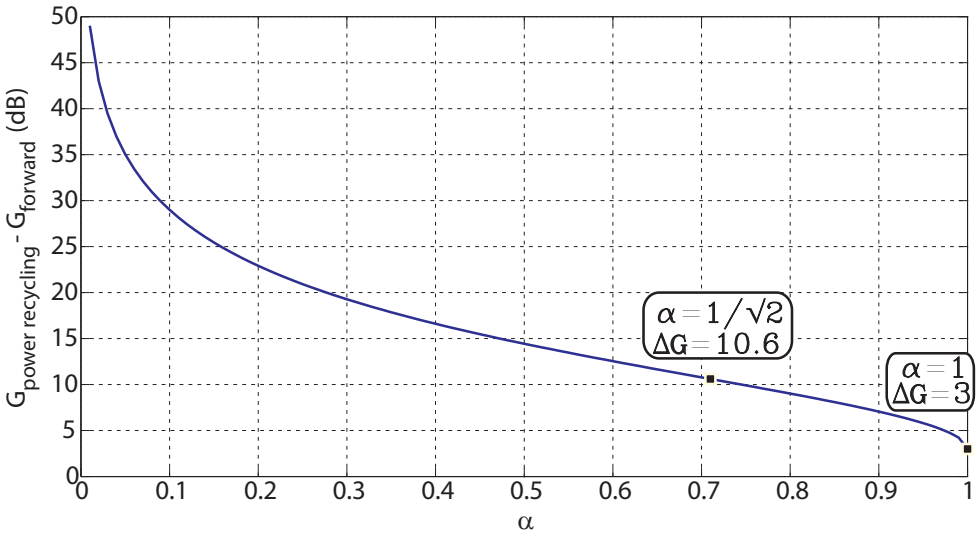


Figure 3.2: Gain increase of the power recycling distributed amplifier in respect to the forward gain of the single-fed configuration as a function of the degree of coupling of the input directional coupler (A) for a single frequency (optimum phase conditions for the maximization of the gain)

$$\theta_{g\_line} + \theta_{aux1} + \theta_{aux2} = \frac{3\pi}{2} + 2\pi m \tag{3.4}$$

m being an integer, and means that the gain is controlled by the coupling of the directional coupler. The gain enhancement as a function of the coupling value A is shown in Fig. 3.2. If, for instance, a 3dB directional coupler is used, the maximum value for the magnitude of b_5/a_6 is 2.42, which represents a 7.6 dB increase in the gain of the overall amplifier, to which the 3 dB from the combination of the output ports must be added. Thus, an increase of 10.6 dB is achieved when compared to the gain of a single-fed configuration (input power injected at port 1, and port 2 terminated in a matched load).

Gain increase can be as high as that desired, Fig. 3.2, at the expense of an extremely low degree of coupling between ports 5 and 6, $A \to 0$, which constitutes a limitation from the implementation point of view. If $A = 1$, there is no coupling between ports 5 and 7, which corresponds to the single-fed feeding (input power injected at port 1, and port 2 terminated in a matched load). In this case, the 3

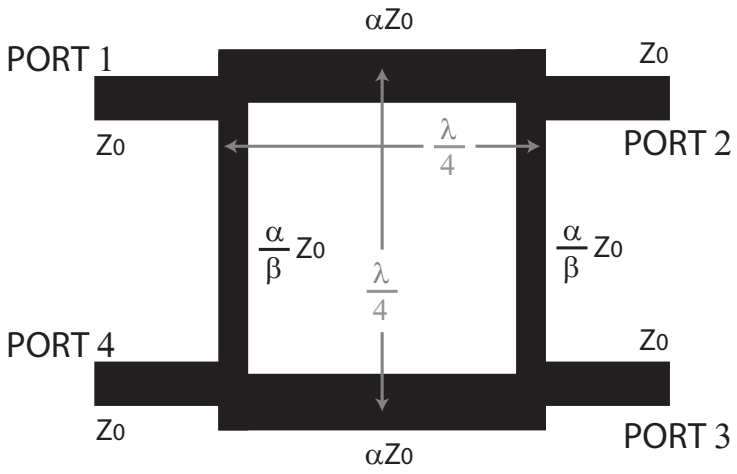


Figure 3.3: 90°-hybrid coupler for arbitrary power divisions

dB gain increase reflected in Fig. 3.2 is, therefore, due to the power combination of ports 3 and 4.

If an ideal and lossless symmetrical coupler (see Fig. 3.3) is used instead of the antisymmetrical one, similar results are obtained. Considering that the S-parameter matrix is given by [39]

$$[S] = -j \begin{bmatrix} 0 & A & -jB & 0 \\ A & 0 & 0 & -jB \\ -jB & 0 & 0 & A \\ 0 & -jB & A & 0 \end{bmatrix}, \quad \begin{matrix} A^2 + B^2 = 1 \\ A, B \in \mathbb{R} \end{matrix} \tag{3.5}$$

The condition for maximum gain can be calculated, and is given by [40]

$$\theta_g + \theta_{aux1} + \theta_{aux2} = \pi + 2\pi m \tag{3.6}$$

m being an integer. Achievable gain levels are identical to those provided by the antisymmetrical directional coupler.

Two main features are, however, responsible for the degradation of the intrinsic amplifier behaviour: losses and mismatch. Both establish a limitation to the maximum achievable gain and to the input match and their effect is assessed in the following subsection.

3.2.2 Effect of mismatch and losses

The intrinsic performance of the proposed amplifier is mainly degraded by the mismatch and the losses associated with the gate transmission line of the basic distributed amplifier.

Firstly, the impact of losses will be analyzed. For this purpose, the gate line is perfectly matched but an attenuation $\alpha_{g\_line}L$ is introduced. The set of S-parameters that define the gate transmission line are now given by $S_{11} = S_{22} = 0$ and $S_{21} = S_{12} = e^{-(\alpha_{g\_line}L + j\theta_{g\_line})}$. If losses are considered, the gain can no longer grow indefinitely but reaches a maximum value that can be obtained by maximizing the b_5/a_6 magnitude. The result indicates that the maximum value for the gain is achieved if phase condition (3.4) or (3.6) is, respectively, imposed for the anti- and the symmetrical cases. In both cases the amplifier remains perfectly matched and there is a value for the degree of coupling, A, that guarantees maximum gain, which is given by [31]

$$A = \sqrt{1 - e^{-2\alpha_{g\_line}L}} \tag{3.7}$$

To evaluate the impact of the mismatch, the distributed amplifier's gate line is assumed to have a characteristic real impedance Z_g, different from Z_0, and an attenuation constant $\alpha_{g\_line}L$. Therefore, a new scattering matrix must be defined for the gate transmission line (see Appendix B).

The analysis of the structure shown in Fig. 3.1 yields the value of the input reflection coefficient b_6/a_6 when the optimum phase shift condition (3.4) or (3.6) is fulfilled. The input match is now, obviously, dependent on the Γ and $\alpha_{g\_line}L$ parameters. The magnitude of the input reflection coefficient as a function of Γ with $\alpha_{g\_line}L$ as a parameter is shown in Fig. 3.4 for a particular value of the coupling ($A = 1/\sqrt{2}$) (see Appendix B). It can be easily inferred from this figure that there is a limit for the gate mismatch and losses that may be tolerated if a particular value for the input match is required. The effect of gate mismatch and losses upon the increase in power gain is shown in Fig. 3.5 for the same value of the coupling ($A = 1/\sqrt{2}$) (see Appendix B). As expected, the power gain decreases as the losses increase. It can be observed in this figure that gate line losses have a greater impact on the amplifier gain than the gate mismatch.

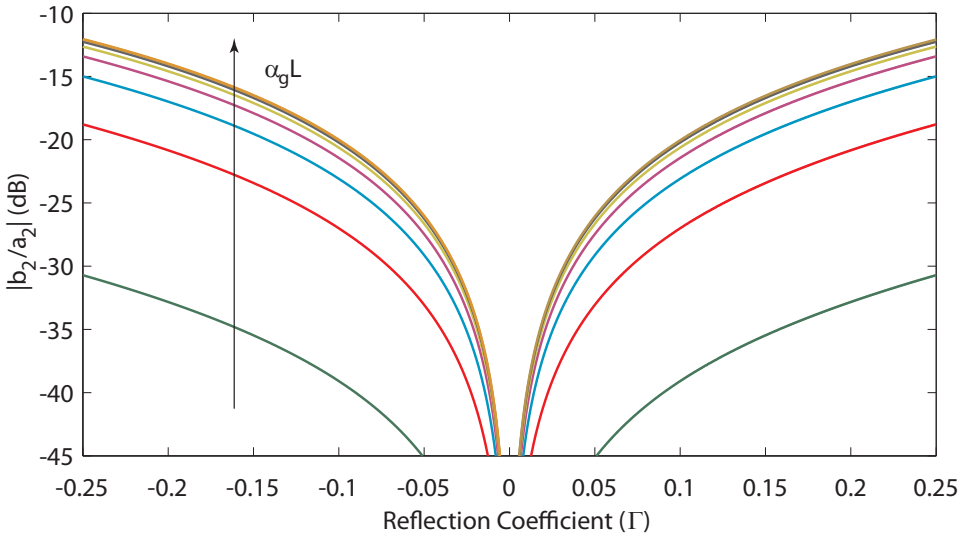


Figure 3.4: Input matching simulation for the power recycling distributed amplifier (3dB directional coupler-based implementation) as a function of Γ and $\alpha_{g\_line}L$ ($\theta_{g\_line} + \theta_{aux1} + \theta_{aux2} = \frac{3\pi}{2}$, $\alpha_{g\_line}L = [0.01, 0.05, 0.1, 0.15, ..., 0.4]$)

Although Figs. 3.4 and 3.5 have been calculated for a 3dB directional coupler, similar information can be obtained for any degree of coupling (see Appendix B). It is worth mentioning that even in the presence of gate mismatch and losses, the increase in the gain level still can be arbitrary, up to a maximum value determined by (3.7), by decreasing the coupling value A accordingly. However, the amplifier input match becomes more sensitive to Γ as A decreases, which imposes a practical limitation to the achievable values of gain and input matching. However, this fact does not avoid the implementation of this novel amplifier concept if a proper design is made.

3.3 Simulation of a 4-stage Power Recycling Distributed Amplifier @$2.8GHz$

To illustrate the previous theory, a 4-stage PRDA has been simulated for an operation frequency of $2.8GHz$ (see Fig. 3.6). The interest of this section relies on the use of non-ideal components that might impact in the previous analysis. Es-

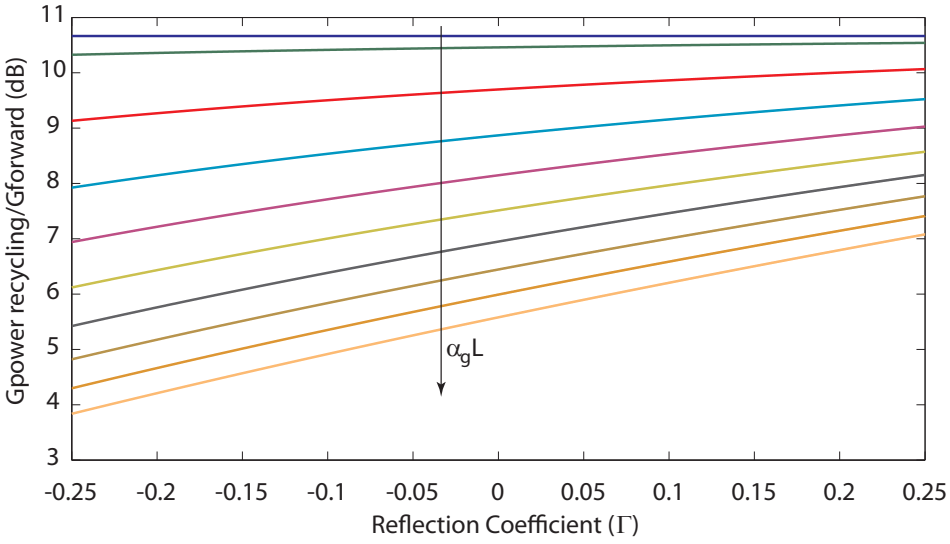


Figure 3.5: Power recycling distributed amplifier gain enhancement versus the forward gain of a generic distributed amplifier (3dB directional coupler-based implementation) as a function of Γ and $\alpha_{g\_line}L$ ($\theta_{g\_line} + \theta_{aux1} + \theta_{aux2} = \frac{3\pi}{2}$, $\alpha_{g\_line}L = [0, 0.01, 0.05, 0.1, 0.15, ..., 0.4]$)

pecially the use of a more realistic model for the active device, that will take into account the feedback between the drain and the gate, is an important step to check the well-functioning of the proposed architecture. In this simulation, the small signal response of the PRDA architecture has been compared to the single- and the dual-fed configurations. The amplifier has been designed in distributed technology (see Appendix A.3). Phase shift between stages for a particular frequency point has been selected according to section 2.3 to achieve optimum load conditions for all the active devices. A PTFE base laminate, RT/Duroid 5880 (h=1.6mm, t=35μm, ε_r=2.2), has been chosen, and the manufacturer's S-parameters of a E-PHEMT Avago transistor, VMMK-1225, have been used.

In Fig. 3.7 the forward and the reverse gain along with the input match for the designed 4-port distributed amplifier is shown. At f_0, 2.8 GHz, $\theta_g = \theta_d = \pi$, and therefore the reverse and the forward gain are coincident. As can be also observed, the simulated input match value for this frequency remains below -20dB. As has been stated earlier this value is of great importance to conduct a successful design (see Fig. 3.4).

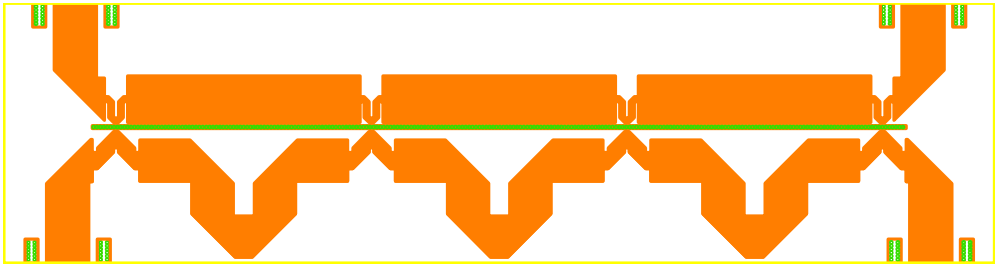


Figure 3.6: Layout for the designed distributed amplifier

Let us first review the simulation of the dual-fed configuration. Fig. 3.8 compares the single- with the dual-fed architecture. The gain and the input match response for both configurations have been superimposed. As predicted by theory it can be seen around a 6dB gain increment at the operation frequency but as a drawback, the poor input match, which is intrinsically unmatched.

Let us now turn to the figures (Figs. 3.9 and 3.10) concerning the PRDA architecture. They show the advantages of the power recycling architecture versus the dual-fed implementation. Figs. 3.9 and 3.10 show, respectively, the power-recycling response using a 3dB 180° and a 90° hybrid ring-based implementation. Slight differences can be viewed between them both, being the 90° hybrid ring-based implementation the one which presents a broader bandwidth. These figures demonstrate that through a proper design it is possible to achieve a important gain enhancement, which is around $10dB$ for this particular selection of the directional coupler, without sacrificing the input match.

The simulations, reassert the results given by the simplified analysis carried out in Section 3.2.1, and demonstrate that this concept works under more realistic conditions. Therefore, it can be concluded that the PRDA is a viable option that could compete with other available alternatives for distributed power combination.

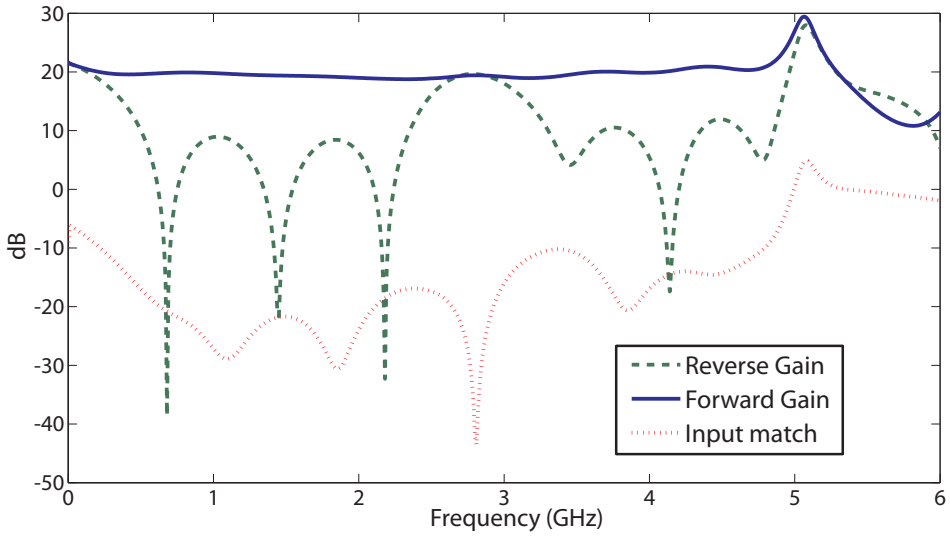


Figure 3.7: Simulated small signal gain (forward and reverse) and input matching for a 4-stage distributed amplifier ($V_{DS} = 3V, I_{DS} = 20mA$)

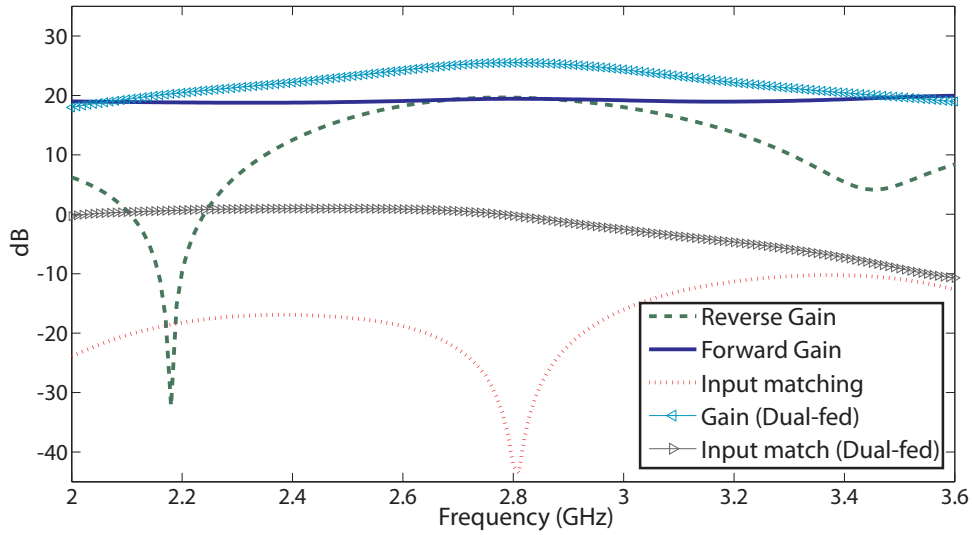


Figure 3.8: Simulated small signal gain (forward and reverse) and input matching for a 4-stage distributed amplifier in single- and dual-fed configuration ($V_{DS} = 3V, I_{DS} = 20mA$)

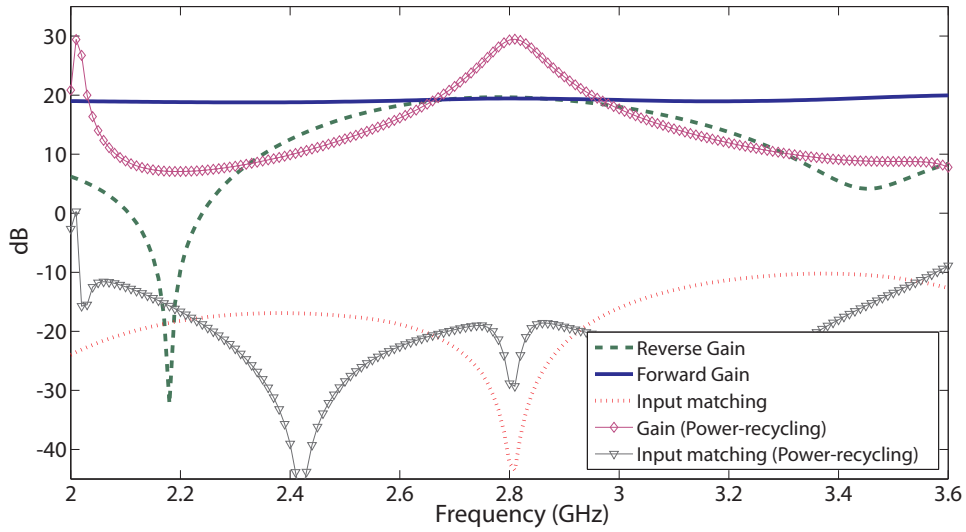


Figure 3.9: Simulated small signal gain (forward and reverse) and input matching for a 4-stage distributed amplifier in single-fed and power recycling (3dB 180° hybrid-based) configuration ($V_{DS} = 3V, I_{DS} = 20mA$)

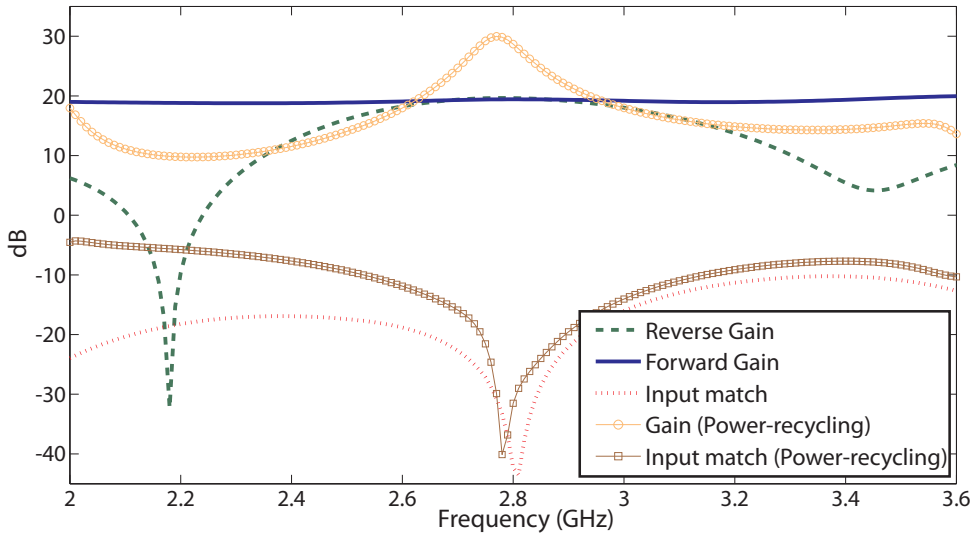


Figure 3.10: Simulated small signal gain (forward and reverse) and input matching for a 4-stage distributed amplifier in single-fed and power recycling (3dB 90° hybrid-based) configuration ($V_{DS} = 3V, I_{DS} = 20mA$)

3.4 Conclusions

The power recycling concept has been used to remove the intrinsic mismatch of the dual-fed distributed amplifier and, at the same time, to enhance the gain. The resulting distributed amplifier structure, called PRDA, can exhibit, through a proper design, enhanced gain, almost perfect input match, and maximum output power under class-A operation within a moderate bandwidth. A simplified analysis of its behaviour has been performed in order to establish its performance limits. From a practical point of view, the main limitations, e.g. mismatch and losses in the gate line, have been identified and assessed.

Chapter 4

Experimental Results

4.1 Introduction

To validate the theory presented in Chapters 2 and 3, a three-stage pHEMT distributed power amplifier based on CRLH unit cells have been manufactured and measured (see Appendix D). The experimental results validate the main conclusions derived from the simplified analysis. These results, that have been published in [16] and [40], are, to the authors' knowledge, the first reference in literature of a distributed power amplifier prototype using CRLH unit cells designed for $\theta = 0$ at the operation frequency. The theory contained in [16] was recently adopted by Fei et al. [41] for the implementation of a 2-D power amplifier for 60 GHz in 65 nm CMOS, thus proving the viability of a metamaterial-based distributed power amplifier design for different technological processes.

The Chapter concludes with the design of a second prototype of a distributed power amplifier in MMIC technology for the uplink Long Term Evolution (LTE) bands ranging from 1.4 to 2.7 GHz, as well as its simulated small- and large-signal performance.

4.2 Prototype 1: pass-band distributed power amplifier (hybrid technology)

The first prototype is a 3-stage distributed power amplifier built using p-HEMT devices (ATF-35143) [16; 42]. For class-A operation the suggested bias point is $I_{DS} = 30mA$, $V_{DS} = 3.0V$, and the estimated optimum load resistance at the intrinsic plane is about 75Ω. Equation (2.19), taking into account this load resistance value and the number of stages, yields the required drain line characteristic impedance: 50Ω. This result allows a 50Ω characteristic impedance for both gate and drain lines.

CRLH TLs were used to reduce circuit size (Fig. 4.6). Both gate and drain unit-cells were made identical and designed to exhibit a zero phase shift ($\theta_g = \theta_d = 0$) at the targeted operation frequency of 1.0 GHz. This condition makes the three devices work with the same load resistance and, thus, deliver the same power. The implementation was carried out on an FR-4 substrate using 0603 lumped components. Input and output capacitances, C_{gs} and C_{ds}, of the active devices were absorbed into the CRLH unit-cells.

4.2.1 Version 1: distributed power amplifier in dual-fed configuration

The first version of the prototype was aimed to verifying the conclusions derived from section 2.3. For this purpose, a dual-fed configuration was mounted with phase shift conditions for optimum power combination. Table 4.1 lists the resulting ideal values of the components for both gate and drain lines, after taking into account the estimated values for C_{gs} and C_{ds}. The lumped components values was chosen as close as possible to the ideal ones. The dual-fed version was built by adding an external power divider and an external power combiner to the single-fed prototype. Divider and combiner losses and mismatch effects were subtracted from the measurements.

Table 4.1: CRLH-TLs ideal values

C_R	L_R	C_L	L_L
1.35pF	3.375nH	7.5pF	18.76nH

A simulation of the small signal gain using the active device's S-parameters has been compared with the measurements. The experimental results are shown in Fig. 4.1, where a reasonable agreement with the simulation predictions can be seen. A significant bandwidth has been obtained, as expected from the design (identical gate and drain transmission lines). In fact, the achievable bandwidth is limited by the cut-off frequencies of both artificial transmission lines, by the frequency response of the reverse gain, and by resonance phenomena associated to the lumped components.

The measured output power as a function of the input power for single-fed and dual-fed configurations are shown in Fig. 4.2. Note the 3 dB shift in the input power level between the dual- and the single-fed prototypes required for a proper comparison of the performance. The results shown in Fig. 4.2 clearly confirm the 3 dB increase in the output power level and the 6 dB increase in the gain in the dual-fed configuration in respect to the single-fed one as predicted by the aforementioned simplified operation theory.

The obtained Power-Added Efficiency (PAE) values are detailed in Fig. 4.3. They are in agreement with the expected values for a class-A amplifier, and suggest that the three devices would be working under similar load conditions. They are also in agreement with those obtained by Eccleston [43] for a dual-fed distributed amplifier based on RH unit-cells designed for $\theta_g = \theta_d = \pi$. The PAE for the dual-fed configuration, as a function of frequency and for a given input power level, is shown in Fig. 4.4. Again, a significant bandwidth is achieved, although the optimum conditions are only fulfilled at one single frequency. The intermodulation distortion ratio performance of both configurations is shown in Fig. 4.5. In this figure the superior performance of the single-fed versus the dual-fed can be observed.

4.2.2 Version 2: distributed power amplifier in power-recycling configuration

This second version of the prototype has been designed to validate, experimentally, the power recycling concept. The design is identical to the first prototype except for the values of the lumped components of the artificial transmission lines that have been slightly modified, while keeping the same operation frequency of 1 GHz. The resulting commercial values for the lumped components used are listed in Table 4.2.

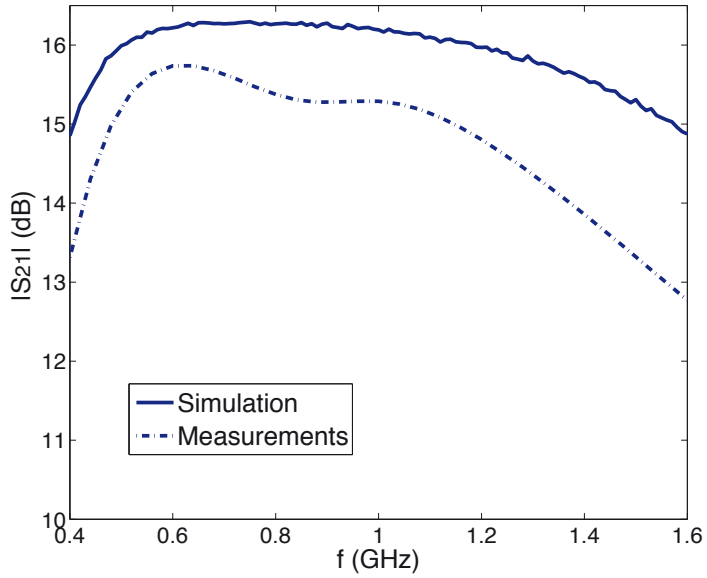


Figure 4.1: Small Signal Gain for a 3-stage CRLH-TL-based dual-fed distributed amplifier ($V_{GS} = -0.3V, V_{DS} = 3V$)

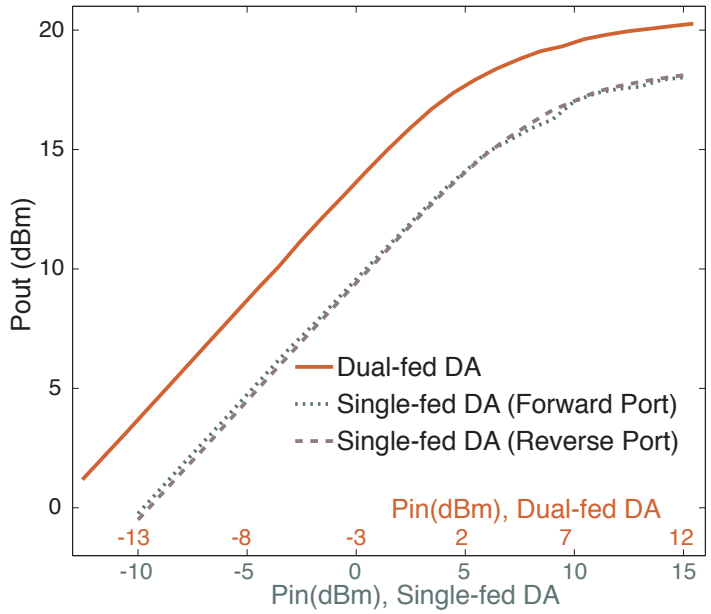


Figure 4.2: Measured Output Power @ 1GHz ($V_{GS} = -0.3V, V_{DS} = 3V$)

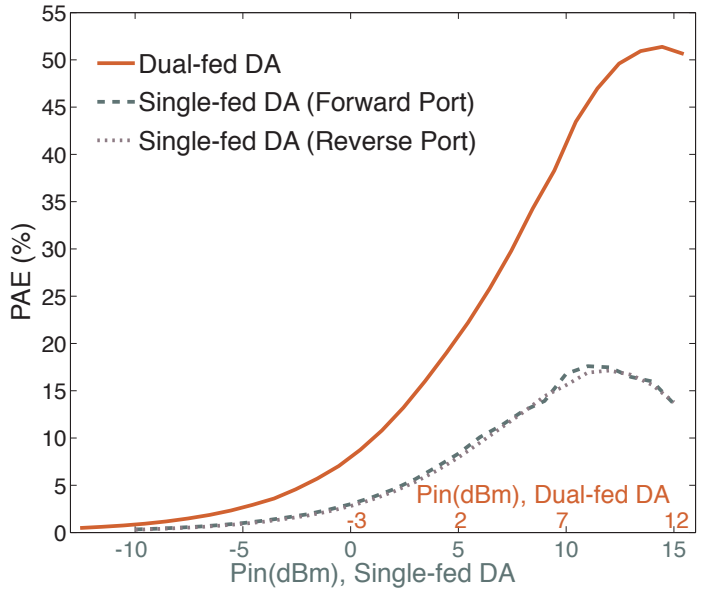


Figure 4.3: Measured Power Added Efficiency @ 1 GHz ($V_{GS} = -0.3V, V_{DS} = 3V$)

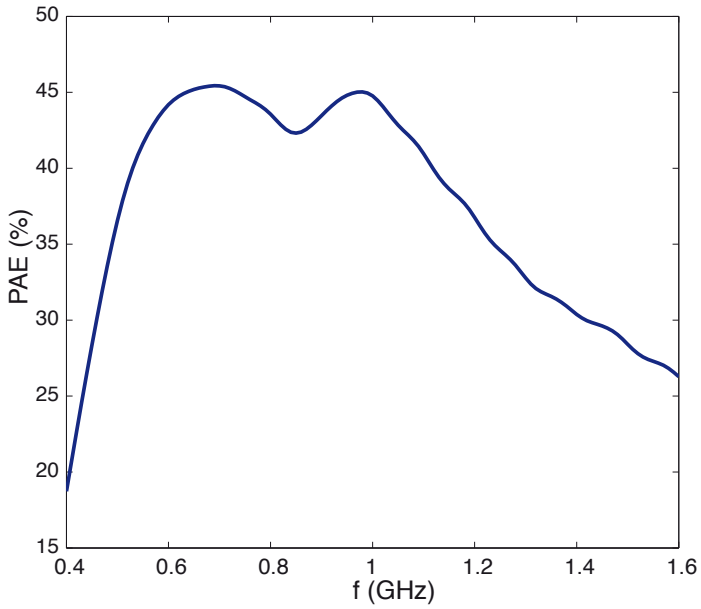


Figure 4.4: Measured Power Added Efficiency versus frequency for a 3-stage CRLH-TL-based dual-fed distributed amplifier ($V_{GS} = -0.3V, V_{DS} = 3V, Pin = 11.5dBm$)

The manufactured distributed amplifier is shown in Fig. 4.7.

Table 4.2: CRLH-TLs commercial values

$C_{R_{gaux}}$	$C_{R_{daux}}$	$L_{R_{g/d}}$	$C_{L_{g/d}}$	$L_{L_{g/d}}$
0.9pF	1.6pF	5.1nH	2.7pF	4.3nH

Firstly, the basic distributed amplifier of Fig. 4.7 was characterized under small-signal conditions. The measured and simulated power gains and input reflection coefficient (in magnitude) are shown in Fig. 4.8. A reasonable good agreement between simulation and experimental results can be observed. The good input match obtained at the design frequency of about 1 GHz is a necessary condition for building a successful PRDA. Notice that there is a drift of 70MHz in the measured frequency for which the input match presents its best performance. These discrepancies between simulations and measurements could be mainly explained through the use of the S-parameters provided by the manufacturer for the active devices, and to tolerances in both active and passive component values.

For illustrative purposes, a 3dB coupling was chosen. Thus, the power recycling version was built by adding an external 180° hybrid both to the input and the output ports of the prototype shown in Fig. 4.7 according to the scheme shown in Fig. 3.1. Notice that this particular coupling value does not provide the maximum increase in the gain. To fulfill the required phase conditions (3.4), two external phase shifters (JSPHS-1000) have been added to ports 1 and 3. For these measurements no losses relative to the external divider, combiner, and physical connectors have been discounted, except for those introduced for the external phase shifters. Measured and simulated power gains and input reflection coefficients for this prototype are shown in Fig. 4.9. The maximum gain is reached for the frequency at which the 4-port device shows its best input match conditions, 1.07 GHz. The measured overall gain enhancement at this frequency is 6 dB compared to the single-fed configuration, which is close to the predicted value (between 7.4 and 7.7 dB), obtained from the simplified analysis performed in the previous section (Fig. 3.5) for $\alpha_{g\_line}L = 0.19$ and $|\Gamma| = 0.05$ (measured values). The input return loss is better than 27 dB around the operating frequency. These two results, the 6 dB gain enhancement and the 27

dB input reflection coefficient demonstrate the viability of the proposed amplifier structure.

Since the prototype has been built by adding external hybrids to the basic distributed amplifier shown in Fig. 4.7, it is possible to compare the performance of the three different possible configurations experimentally: single-fed, dual-fed and power recycling. The small-signal performance of these three amplifiers is shown in Fig. 4.10. It is worth emphasizing that the highest gain value with simultaneous good input match is provided by the power recycling distributed amplifier.

The output power at the 1dB gain compression point (P1dB) provided by the manufacturer for one single device at the chosen bias point is around 14 dBm. If three devices were perfectly combined, the expected value for P1dB would be 14dBm + 4.8 dB = 18.8 dBm. The measured output power at the P1dB for the 3-stage prototype is 18 dBm (Fig. 4.11), and the power added efficiency of the amplifier structure at the frequency of 1.07GHz is around 27% for the P1dB, which suggests that the three devices are working under similar conditions and close to optimum class-A operation.

To evaluate the linearity exhibited by the power recycling version, the intermodulation distortion ratio has been measured and compared to the single-fed amplifier presented in [16]. The distortion properties are expected to be the same, since the same active devices and frequency of operation were selected in both prototypes. In Fig. 4.12 both responses have been superimposed. Note that the input power axis must be shifted to provide a fair comparison, which should be referenced to the same output power level. The results highlight that there is no tradeoff between the increase in gain and a deterioration in the linearity performance.

Measurements of modulated signals, taken with the aid of the Agilent 89600 VSA Software, have also been made, providing an idea of the linearity of the amplifier when it works under a more complex modulation scheme. Figs. 4.13, 4.14 and 4.15 show the amplified modulation schemes for a 4FSK, an EDGE and a GSM signal, respectively, when the amplifier is working at the 1dB compression point. All the measurements show a good linearity, the EVM being below 1% in all cases.

Summarizing, the comparison with the large signal performance of the single-fed and dual-fed configuration, which was detailed in [16], shows that the power recycling distributed amplifier is the only implementation that can optimally combine

the output power of an arbitrary number of active devices with simultaneous input match and an arbitrary gain level. The bandwidth reduction is thus traded for a boost in gain and output power performance. This might be of interest at very high frequency ranges where available power is very low, and hence could compete with other existing output power combination techniques. However, because working at higher frequency ranges is more critical due to the associated increase in cost, losses and coupling between elements, the MMIC technology is almost mandatory. Recently, Fei *et al.* [41] presented a 60-GHz power amplifier in 65-nm CMOS technology based on a CRLH-TL-based zero phase shifter. In this work the authors highlight the most important problems associated with the increase in frequency. As they mention, for this frequency range, CRLH-TLs can no longer be assumed as ideal due to the large parasitics of the transistors, so losses and phase error must be carefully studied to prevent a severe degradation in the amplifier performance. The analysis shows that as the number of stages increases, so does the power gain degradation, thus both the losses and the phase error limit the maximum number of stages that can be implemented. On the other hand, in the millimeter-wave frequency region, the lumped capacitor and inductor to build the CRLH-TL are more compact and less lossy, therefore the on-chip implementation in the CMOS process is feasible [41]. Furthermore, additional control over the active devices is gained, since their periphery is designable, which could be useful when meeting the load requirements of the designable characteristic impedances of the artificial transmission lines.

4.3 Prototype 2: a MMIC 3-stage pass-band distributed power amplifier

The design of an MMIC distributed power amplifier for the uplink Long Term Evolution (LTE) bands ranging from 1.4 to 2.7 GHz, as well as its simulated small- and large-signal performance, are presented [44; 45].

The ED02AH process of the OMMIC foundry for MMICs has been selected for the amplifier design. This process works up to millimeter-wave bands, and can integrate PHEMT devices both in the depletion or the enhancement mode. Balanced

CRLH-TLs have been used for the gate and drain lines to achieve a band-pass response [16]. The characteristic impedance for both transmission lines has been set to 50Ω, which avoids the need for an impedance transformer and the subsequent reduction in the practical bandwidth. Once the characteristic impedances of the gate and the drain line and the total number of active devices are set, the physical characteristics of the active device, the gate width, W_u, and the number of fingers, N_{bd}, must be selected to provide optimum load conditions. The bias point, corresponding to a class-A mode, has been set to $V_{gs} = 0V$ and $V_{ds} = 4.75V$. For the active device, which works in the depletion mode, $W_u = 35\mu m$ and $N_{bd} = 6$ have been chosen. The total number of active devices is $N = 3$, which gives $R_L = 75\Omega$. The operation frequency, $f_0 = 1.9GHz$, has been selected to cover the LTE frequency bands ranging from 1.4 GHz to 2.7 GHz. The phase shift between stages is 0 @ f_0 for both gate and drain transmission lines. The circuit size is 2 mm x 3 mm. The layout is shown in Fig. 4.16. The amplifier behaviour can be improved in terms of output power and efficiency by combining both output ports by means of a Wilkinson power combiner. Simulations have been carried out using a lossless Wilkinson power combiner at the drain ports.

4.3.1 Small Signal Simulations

Both small and large signal simulations have been carried out using the Microwave Office CAD tool. The components library provided by OMMIC has been used for circuit simulations. For the electromagnetic simulations, the $AXIEM^{TM}$ simulator, based on the method of moments, has been used. All the layers detailed in the OMMIC process have been included for this task. The resulting artificial lines S-parameters have been connected to the small signal model for the active device for the comparison with circuit simulations. Fig. 4.17 shows the forward and reverse gain for the 4-port distributed amplifier between 1 and 3 GHz. The gain level varies between 11.5 and 13 dB for the frequency range between 1.4 and 2.7 GHz. The input matching is below -15 dB for the band of interest. The amplifier response when a Wilkinson output combiner is used is also shown. The expected increase of 3 dB gain is clear in the figure. Circuit simulations are compared to electromagnetic results (dashed lines in the same color) showing a close agreement between both of

them.

4.3.2 Large Signal Simulations

The previous circuit simulations with the large signal model of the active device provided by OMMIC have been used for the CW large signal simulations. The solution has been found using the harmonic balance method. Fig. 4.18 shows the output power, the large-signal gain, and the efficiency for the operating frequency, f_0. The 1 dB compression point, CP-1dB, is reached for an 8.5 dBm input level. The output power for this point is 23.6 dBm. LTE specifies an output power $\leq$ 24 dBm for a Local Area Base Station (BS) and an output power $\leq$ 20 dBm for a Home BS (or one transmit antenna port). The drain efficiency is around 21.4% for the CP-1dB and around the 30% for the compression. Since several LTE operating bands are expected to be covered, it is interesting to check the amplifier′s response versus frequency. Fig. 4.19 shows the output power and the efficiency for the CP-1dB. The output power requirement for LTE is fulfilled, and the PAE is above 16% for the whole frequency range. Finally, the load lines for the three active devices have been compared. They are all very similar for the whole frequency range, achieving their top resemblance at 1.7 GHz. In Fig. 4.20 the load lines are compared for this frequency at the CP-1dB. Those results guarantee the equal contribution of the three active devices, and thus corroborate the theory presented in [16].

4.3.3 LTE Frequency Division Duplexing Simulations

In order to have a preliminary evaluation of the amplifier performance for LTE signals some simulations have been carried out using the signal generator available in Microwave Office. The results have been obtained using the time domain Visual System Simulator (VSS). Fig. 4.21 shows the input and output power spectrum. The spectral regrowth produced by the amplifier can be characterized with the Adjacent Channel Power Ratio (ACPR). In Fig. 4.22 the ACPR versus the output power for different interfering adjacent channel offsets is plotted for an E-UTRA interface with a 10 MHz channel bandwidth. The E-UTRA channel is compared to the corresponding adjacent E-UTRA and UTRA channels detailed in the LTE communication standard. The modulation type is QPSK. According to the LTE

specifications the ACPR must be below -44.2 dB. The specifications are satisfied whenever the output power is below 16dBm.

4.4 Final remarks

In this Chapter, two distributed power amplifier designs have been presented to corroborate the theory previously exposed.

The first prototype shows a particular optimum design, defined by $\theta_g = \theta_d = 0$ at the operation frequency and the use of CRLH unit cells, which has been used to demonstrate the viability of this structure as an optimum class-A power amplifier combiner. A three-stage p-HEMT prototype has been manufactured and measured.

The experimental results of the first version of the prototype have confirmed the main conclusions derived from a simplified analysis (intrinsic performance). In particular, it has been shown that it is possible to obtain the maximum power from a given number of active devices under class-A operation with significant gain values through the use of CRLH unit cells and dual-fed distributed amplifier topology.

In the second version of the prototype problems concerning the input match have been solved, following the theory of Chapter 3. A PRDA prototype has been designed, built and measured. The experimental results obtained as regards gain, input match, output power, efficiency and bandwidth demonstrate the validity of the simplified analysis and the potential of the PRDA as an optimum active class-A power combiner.

Finally, a band-pass MMIC distributed power amplifier design for LTE applications has been described with the aim of migrating towards to monolithic technology. Small signal simulations show a good agreement between circuit and EM simulations. The load lines of the three active devices suggest that they are working under very similar conditions and therefore delivering the same power to the output port. The simulated output power for a CW input signal fulfils LTE specifications for the uplink channels ranging from 1.4 to 2.7 GHz. Lastly, preliminary results concerning the amplifier's behaviour under an LTE FDD signal have also been assessed. The simulated results obtained are encouraging for a future physical implementation.

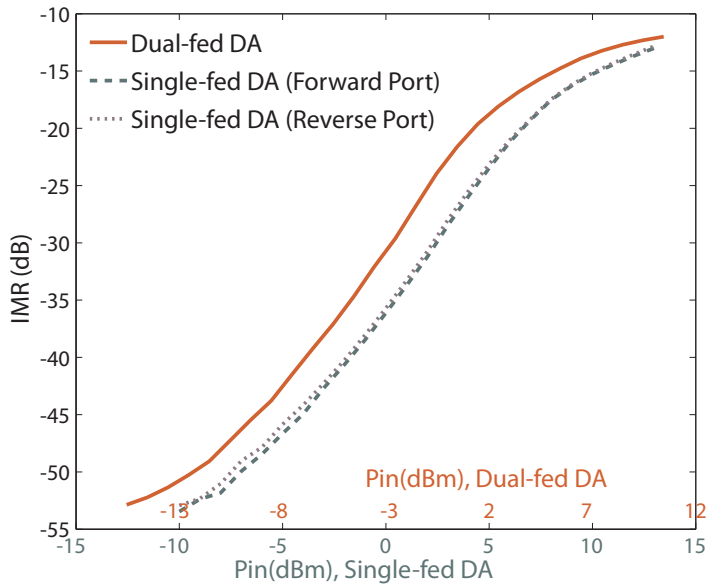


Figure 4.5: Measured Intermodulation Distortion Ratio @ 1 GHz ($V_{GS} = -0.3V, V_{DS} = 3V$, two-tone test $\Delta f = 1MHz$)

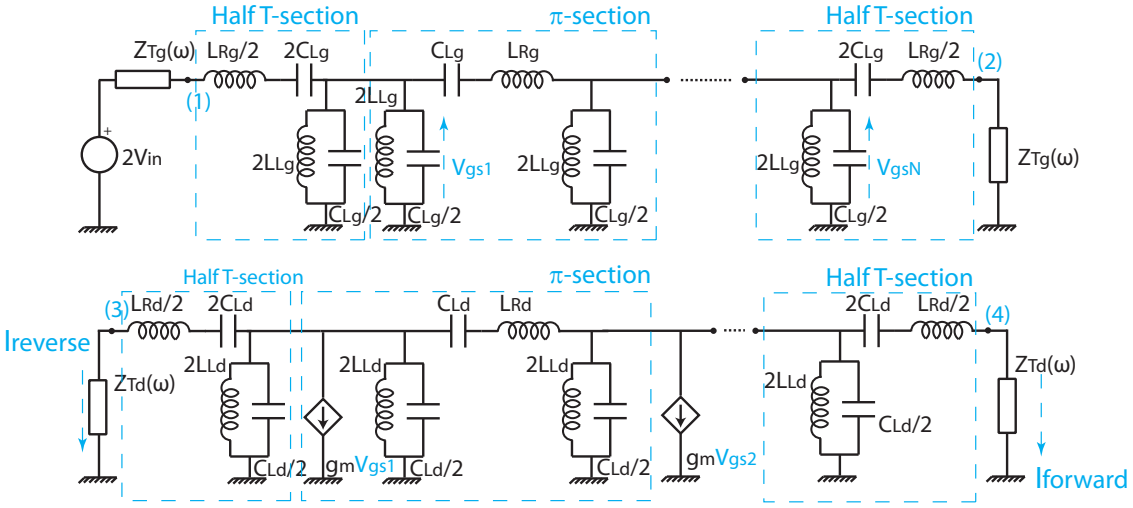


Figure 4.6: Generic CRLH TL-based distributed amplifier

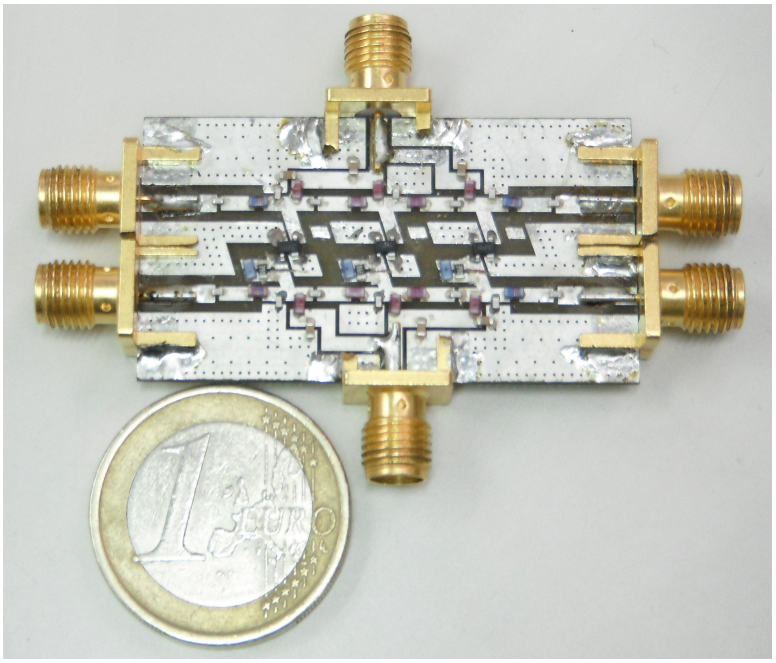


Figure 4.7: CRLH TL-based distributed amplifier prototype (hybrid technology)

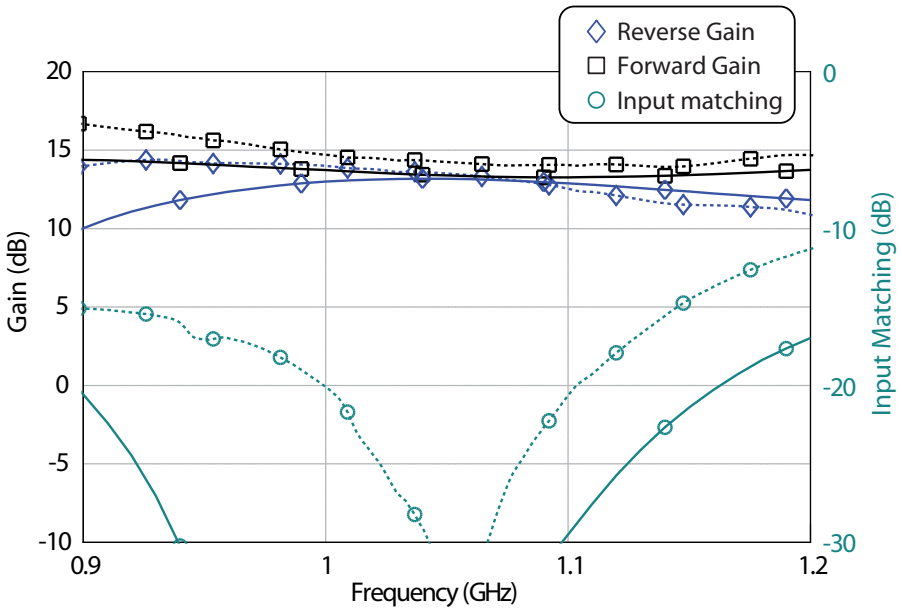


Figure 4.8: Simulated (solid line) and measured (dashed line) small signal gain (forward and reverse) and input matching for a 3-stage CRLH-TL-based distributed amplifier ($I_{DS} = 30mA$; $V_{DS} = 3V$)

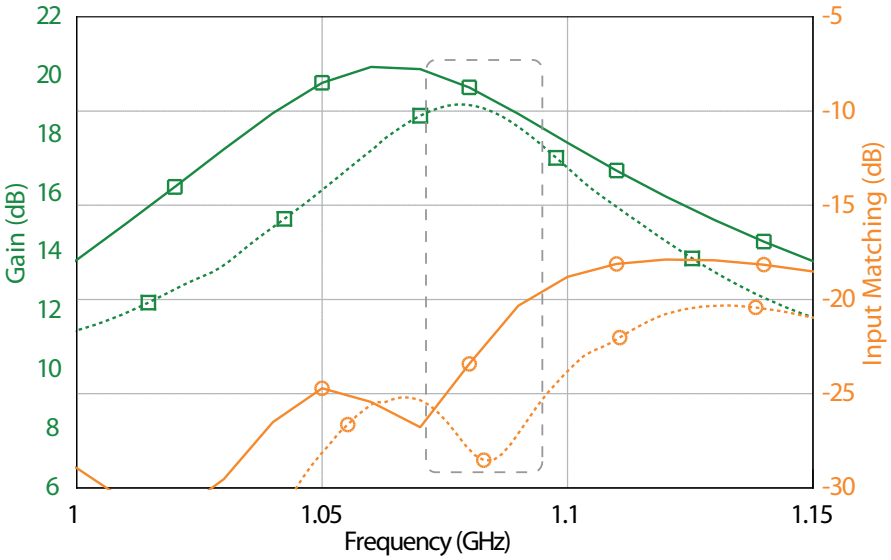


Figure 4.9: Simulated (solid line) and measured (dashed line) small signal gain and input matching for a 3-stage power recycling CRLH TL-based distributed amplifier ($I_{DS} = 30mA$; $V_{DS} = 3V$)

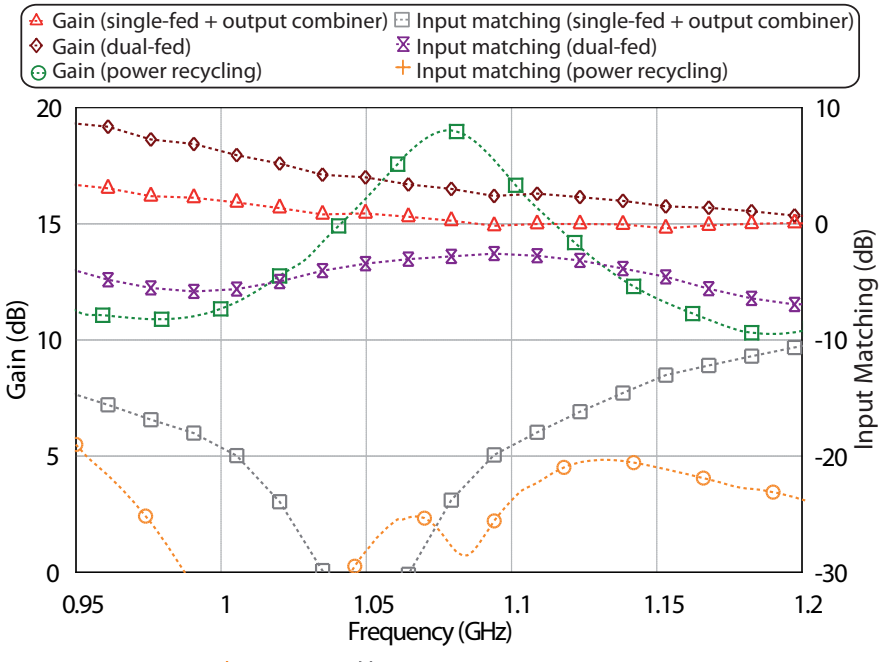


Figure 4.10: Measured small signal gain and input matching for three different 3-stage CRLH-TL-based distributed amplifiers (Bias point: $V_{DS} = 3V$; $I_{DS} = 30mA$)

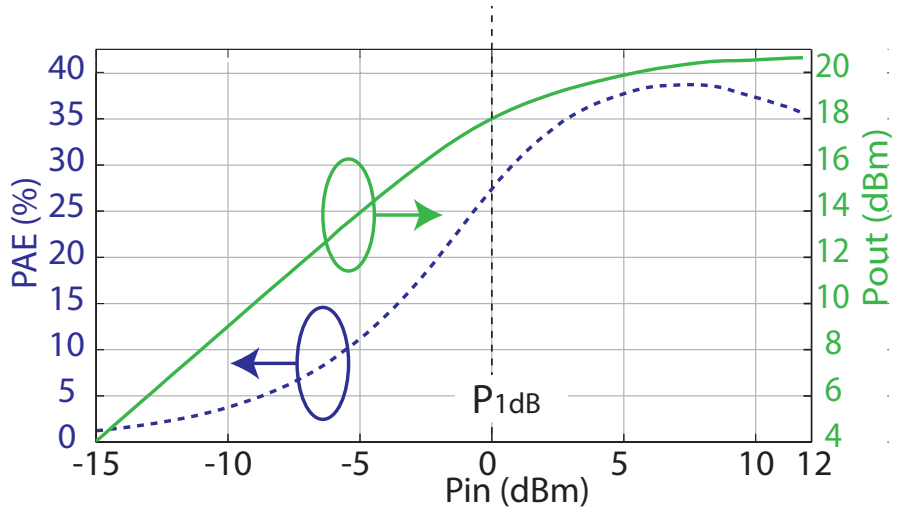


Figure 4.11: Measured power added efficiency (dashed line) and output power (solid line) for the 3-stage CRLH-TL-based power recycling distributed amplifier ($I_{DS} = 30mA$; $V_{DS} = 3V$) @ $f_0 = 1.07GHz$

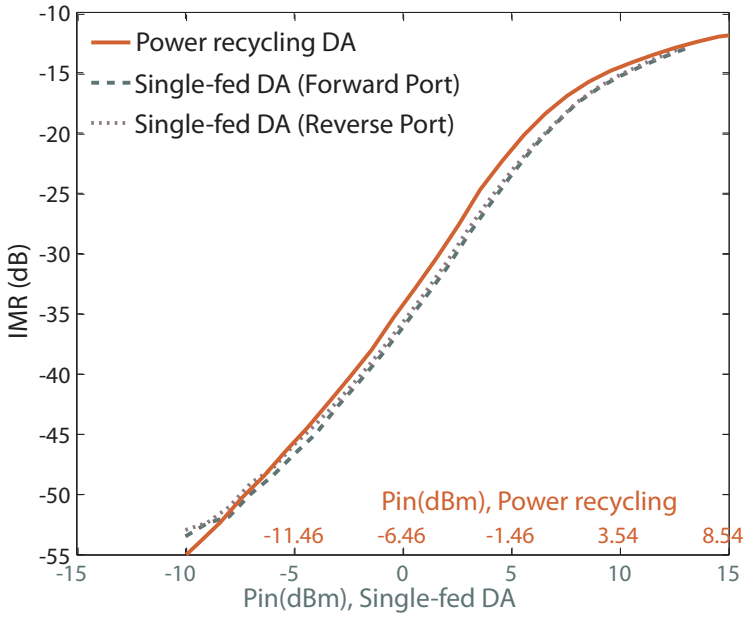


Figure 4.12: Comparison of the measured intermodulation distortion ratio of the power recycling DA versus the single-fed DA ($I_{DS} = 30mA$, $V_{DS} = 3V$, two-tone test $\Delta f = 1MHz$, $f_0 = 1.07GHz$)

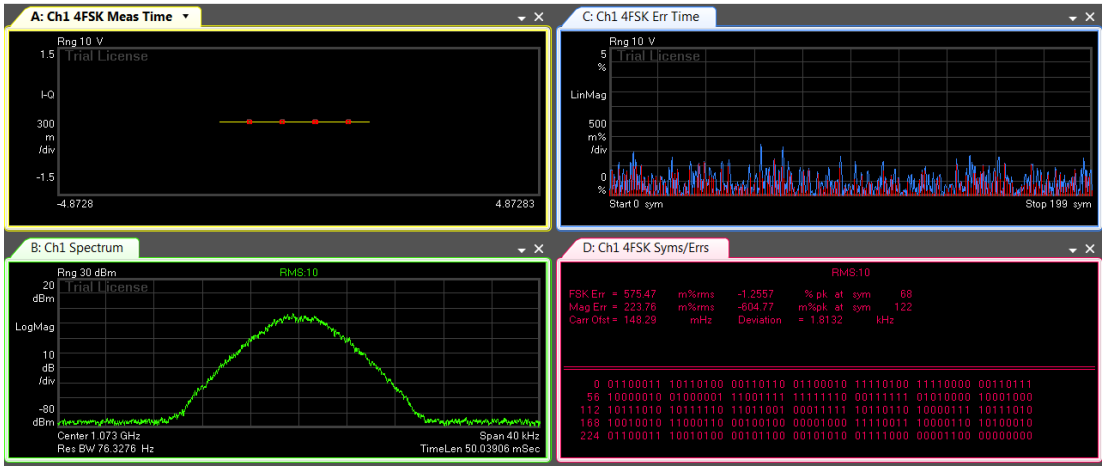


Figure 4.13: Amplified 4FSK signal @ P1dB

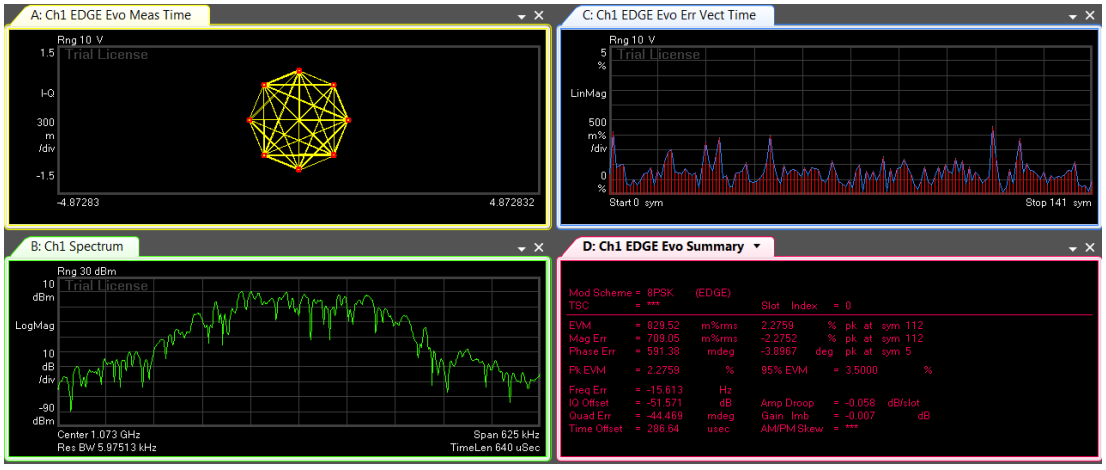


Figure 4.14: Amplified EDGE signal @ P1dB

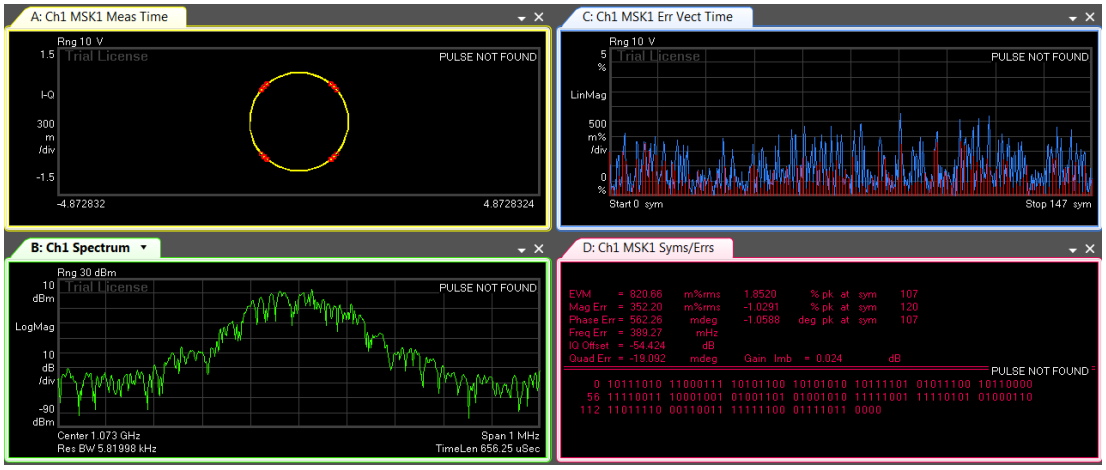


Figure 4.15: Amplified GSM signal @ P1dB

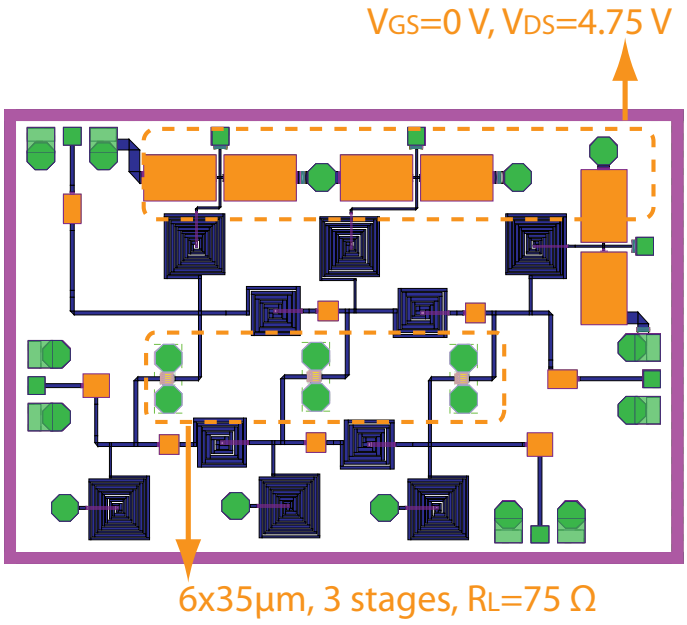


Figure 4.16: Distributed amplifier's layout (access ports highlighted).

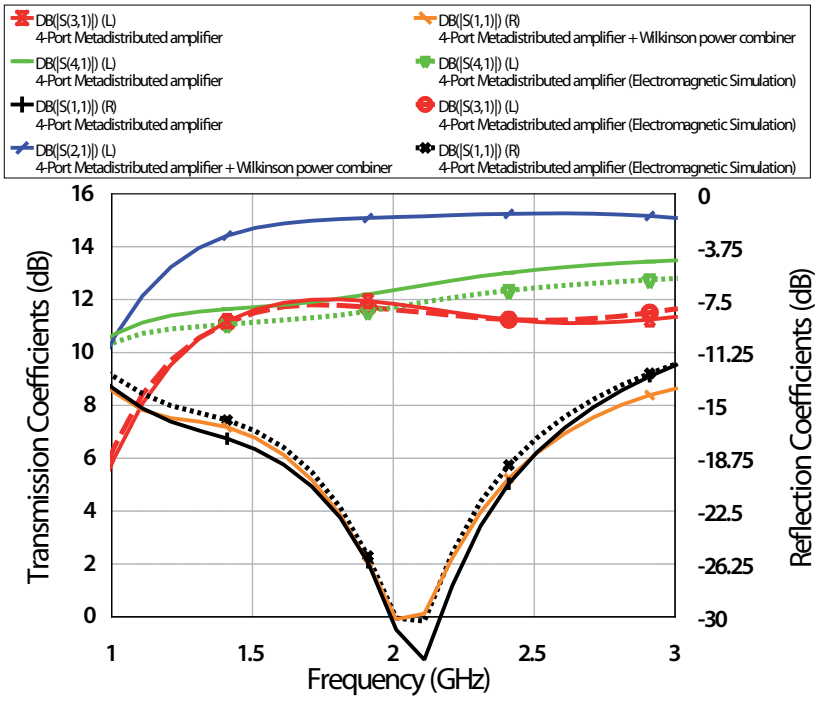


Figure 4.17: Circuital (solid line) and electromagnetic (dashed line) S-parameters simulation.

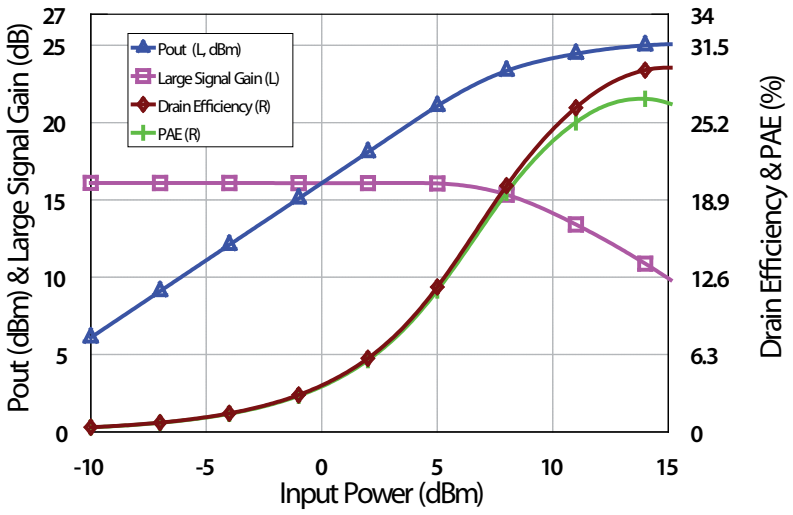


Figure 4.18: Simulated output power (blue), large signal gain (purple), drain efficiency (brown) and PAE (green) f_0.

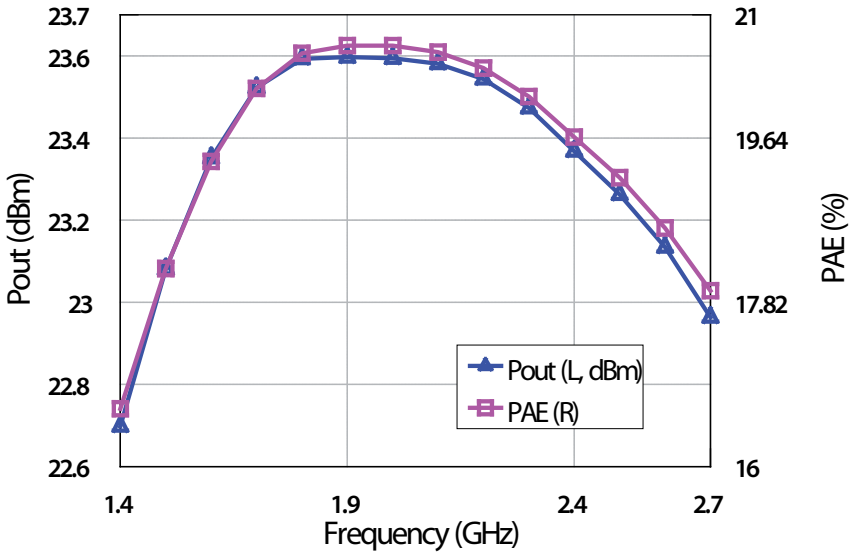


Figure 4.19: Simulated output power (blue), PAE (purple) versus frequency @ CP-1dB=8.5 dBm.

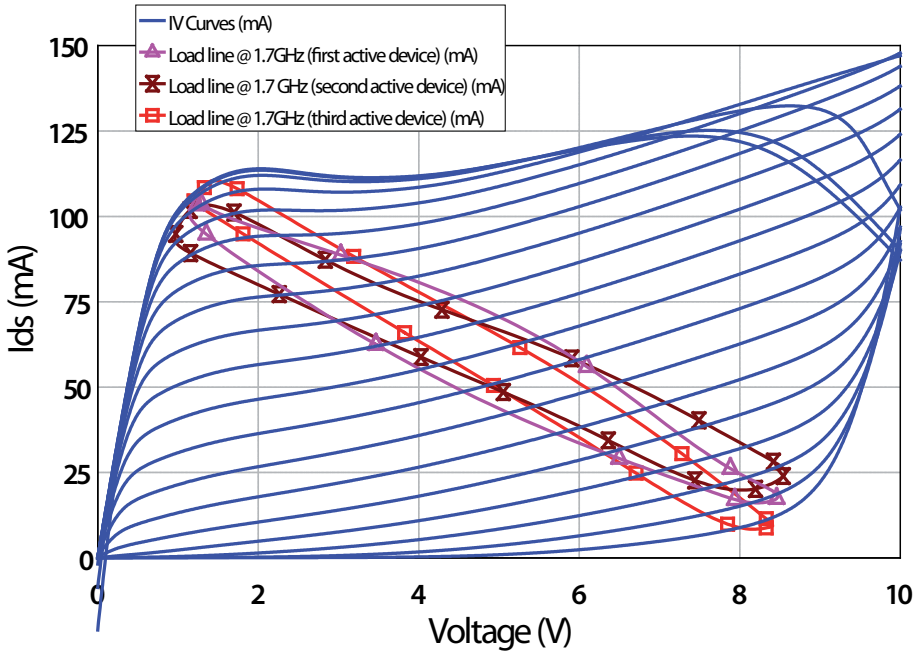


Figure 4.20: Load lines for the three active devices @ 1.7 GHz for the CP-1dB.

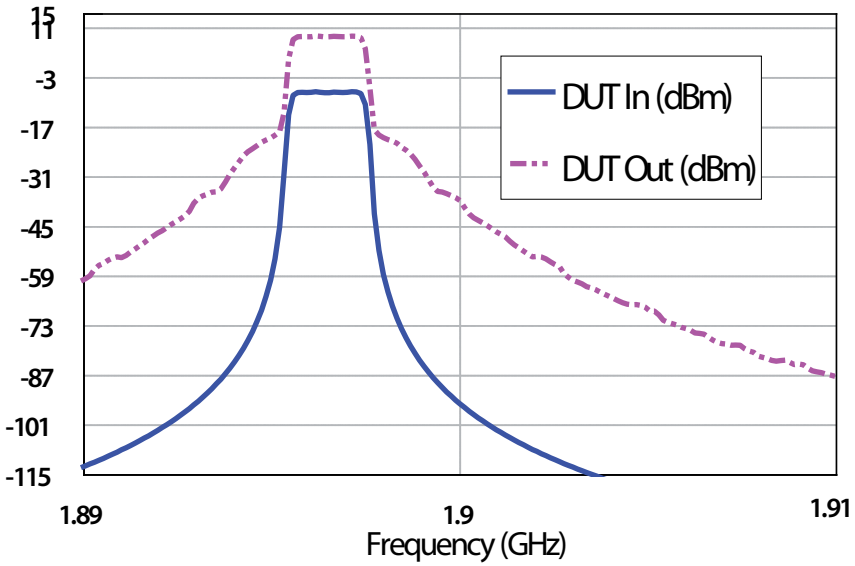


Figure 4.21: Simulated input and output power spectrum, LTE FDD signal @ 1.9 GHz.

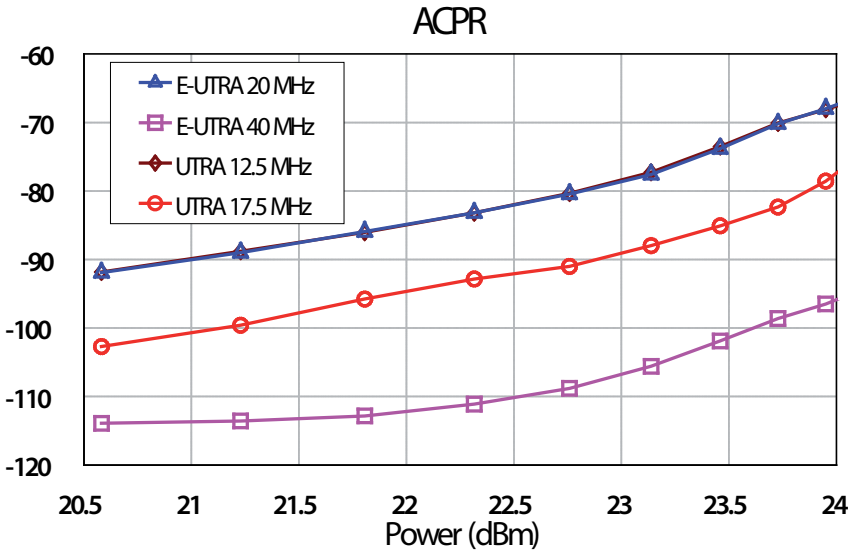


Figure 4.22: Simulated ACPR for different interfering channels for an LTE FDD signal @ 1.9 GHz.

Chapter 5

High efficiency distributed power amplifier design

5.1 Introduction

So far, a class A bias point has been considered for the distributed power amplifier design theory developed in previous chapters. Class A guarantees a very good linearity performance at the expense of a low efficiency. This approach is usually adopted when a conventional broadband distributed amplifier is the aim of the design, since the peak-to-average power ratio (PAPR) is limited. The power recycling distributed amplifier configuration is, however, more suitable to be used as a power amplifier, since it can be designed to deliver to the output all the available power of the active devices. It is, therefore, of interest to consider the different strategies that might increase their efficiency at the expense of a decrease in linearity.

In this chapter, firstly, the classic theory for power amplifier design is reviewed. It is important to identify the harmonic load impedances that might be of interest in order to achieve a proper waveform shaping. In the second section of the chapter there is a discussion about the options for a distributed amplifier design in conjunction with high efficiency power amplifier topologies. The conclusions derived from the analysis of the intrinsic power performance of distributed amplifiers allow an easy identification of the high efficiency modes that can be synthesized in a distributed structure, and thus different alternatives for high efficiency design

Table 5.1: Conduction Angle Modes.

Mode	*Conduction Angle* (α)	*Maximum efficiency*
A	2π	50%
AB	$\pi - 2\pi$	$50\% - 78.5\%$
B	π	78.5%
C	$0 - \pi$	$> 78.5\%$

are presented. The last part of the chapter presents a power recycling distributed amplifier design example using a GaN active device in Class AB.

5.2 Power amplifier theory for high efficiency modes of operation

Firstly the conventional high efficiency modes of operation will be detailed. Secondly the overdriven power amplifiers and the Class F mode will be introduced. Finally, the switching mode power amplifiers will be studied.

5.2.1 Conventional High Efficiency Amplifier Modes

The analysis of the conventional Class AB, Class B and Class C configurations is based on the reduction of the conduction angle of an RF power device. For this reason the bias point must be shifted from the middle of its linear region (Class A) towards a low quiescent current point (Fig. 5.1) [46]. By doing so, the transistor will be able to reach the pinch-off or the cut-off region, which never happens for a Class A operation for moderate power levels. For Class B operation the active device will be pinched-off or cut-off for one half of the signal period. Class AB is between Class A and Class B, that is, the active device is pinched-off or cut-off for less than one half of the signal period. Finally, for a Class C the conduction angle is less than π. Table 5.1 summarizes the different conduction angle modes and their corresponding maximum efficiencies. Looking at Fig. 5.1 it is evident that the DC supply will decrease as the conduction angle is reduced, which explains the improvement related to the efficiency.

The analysis of the performance of the classic modes of operation can be com-

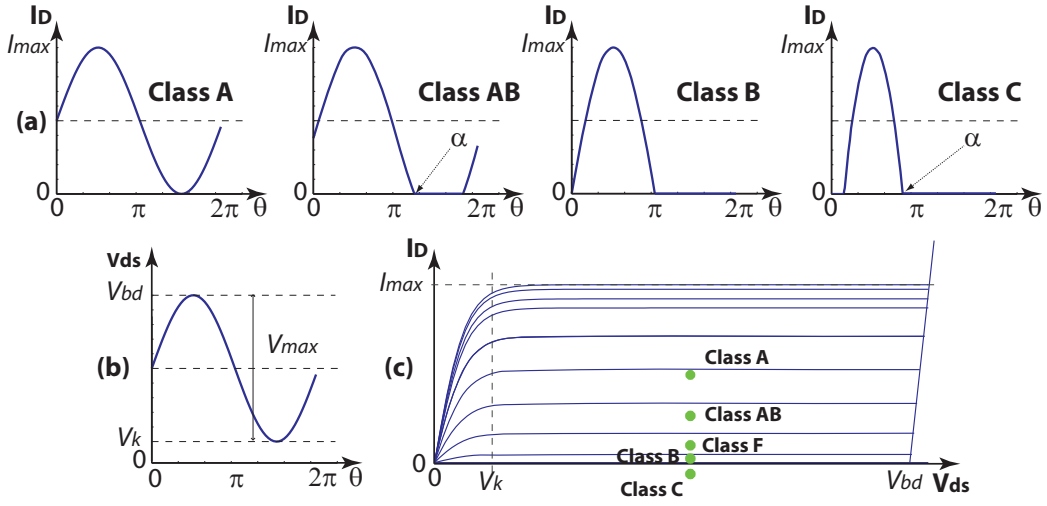


Figure 5.1: Current (a) and voltage (b) waveforms, and bias points (c) for the conventional high efficiency amplifier modes.

puted by defining the output current and voltage waveforms that are expected to be synthesized. Equations (5.2) and (5.3), where $\theta = \omega t$ and α is the drain Current Conduction Angle (CCA), define the waveforms depicted in Fig. 5.1.

$$i_D(\theta) = \begin{cases} I_{dc} + I_{pk} \cdot \cos\theta & \text{if} -\alpha/2 \leq \theta \leq \alpha/2 \\ 0 \quad \text{otherwise} \end{cases} \tag{5.1}$$

being $I_{pk} = I_{max} - I_{dc}$, and $\cos(\alpha/2) = -\dfrac{I_{dc}}{I_{pk}}$, so

$$i_D(\theta) = \begin{cases} \dfrac{I_{max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) & \text{if} -\alpha/2 \leq \theta \leq \alpha/2 \\ 0 \quad \text{otherwise} \end{cases} \tag{5.2}$$

$$v_{DS}(\theta) = V_{dc} - \frac{V_{max}}{2} \cdot \cos\theta \tag{5.3}$$

To evaluate its performance in terms of output power, efficiency and optimum load conditions it is convenient to expand the output and voltage waveforms into its Fourier series coefficients, (5.4) and (5.5),

$$i_D(\theta) = \sum_{n=0}^{\infty} I_n \cos(n\theta) \tag{5.4}$$

$$v_{DS}(\theta) = \sum_{n=0}^{\infty} V_n \cos(n\theta) \tag{5.5}$$

whose expansion coefficients V_n are given by:

$$V_n = \begin{cases} V_{dc} & n = 0 \\ -\dfrac{V_{max}}{2} & n = 1 \\ 0 & n \geq 2 \end{cases} \tag{5.6}$$

and the expansion coefficients I_n by:

$$I_0 = \frac{1}{2\pi} \int_{-\alpha}^{\alpha} \frac{I_{max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2))\, \mathrm{d}\theta \tag{5.7}$$

$$I_n = \frac{1}{\pi} \int_{-\alpha}^{\alpha} \frac{I_{max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cos(n\theta)\, \mathrm{d}\theta \tag{5.8}$$

$$I_n = \begin{cases} \dfrac{I_{max}}{2\pi} \cdot \dfrac{2 \cdot \sin\left(\frac{\alpha}{2}\right) - \alpha \cdot \cos\left(\frac{\alpha}{2}\right)}{1 - \cos\left(\frac{\alpha}{2}\right)} & n = 0 \\ \dfrac{I_{max}}{2\pi} \cdot \dfrac{\alpha - \sin(\alpha)}{1 - \cos\left(\frac{\alpha}{2}\right)} & n = 1 \\ \dfrac{2 \cdot I_{max}}{\pi} \cdot \dfrac{\sin\left(n \cdot \frac{\alpha}{2}\right) \cdot \cos\left(\frac{\alpha}{2}\right) - n \cdot \sin\left(\frac{\alpha}{2}\right) \cos\left(n \cdot \frac{\alpha}{2}\right)}{n \cdot (n^2 - 1) \cdot \left[1 - \cos\left(\frac{\alpha}{2}\right)\right]} & n \geq 2 \end{cases} \tag{5.9}$$

The DC, the fundamental, and the second and third harmonics of the drain current as a function of the CCA are depicted in Fig. 5.2. Using the Fourier coefficients it is easy to obtain the optimum load at the different harmonics, Z_n, the DC power, P_{DC}, the output power at different harmonics, $P_{RF,n}$ the drain efficiency, η, and the power added efficiency, PAE, which are given by the following expressions [47]:

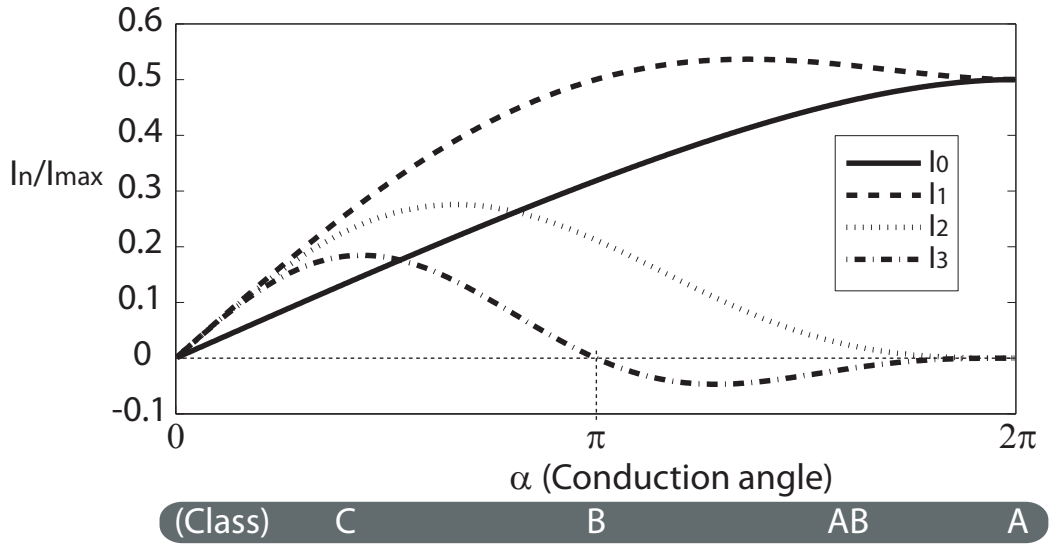


Figure 5.2: Fourier coefficients normalized to the device maximum current, I_{max}, as a function of the conduction angle, α.

$$Z_n = -\frac{V_n}{I_n} = \begin{cases} \dfrac{V_{max}}{I_{max}} \cdot \pi \cdot \dfrac{1 - \cos\left(\dfrac{\alpha}{2}\right)}{\alpha - \sin(\alpha)} & n = 1 \\ 0 \quad n \geq 2 \end{cases} \tag{5.10}$$

$$P_{DC} = I_0 \cdot V_0 \tag{5.11}$$

$$P_{RF,n} = \frac{I_n \cdot V_n}{2} \tag{5.12}$$

$$\eta = \frac{P_{RF,1}}{P_{DC}} \tag{5.13}$$

$$PAE = \frac{P_{RF,1} - P_{IN}}{P_{DC}} \tag{5.14}$$

The load resistance at the fundamental frequency, the DC power consumption, and the RF output power at the fundamental frequency, normalized to the Class A mode ($\alpha = 2\pi$), as a function of the CCA have been plotted in Figs. 5.3, 5.4, 5.5. The drain efficiency versus α has been detailed in Fig. 5.6.

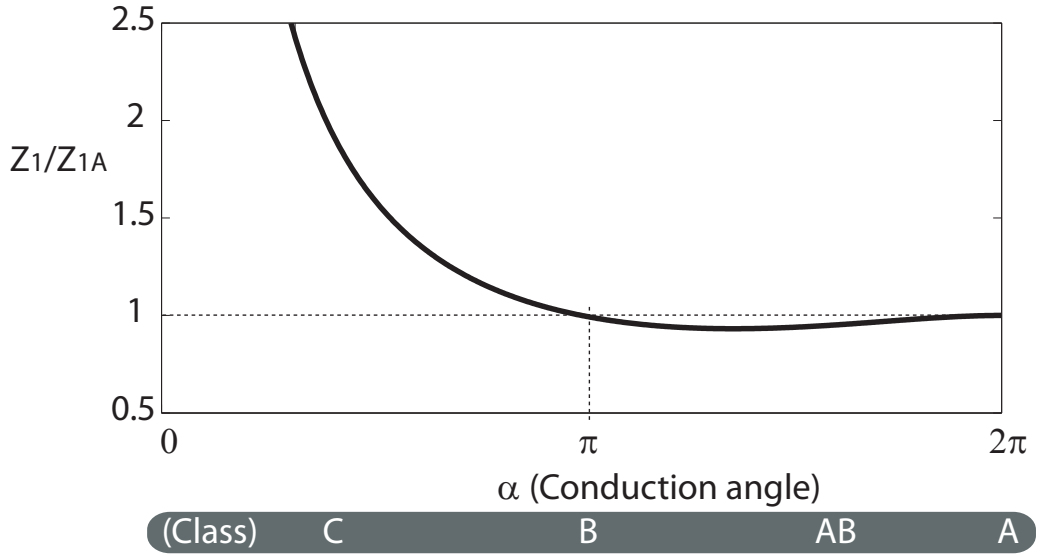


Figure 5.3: Optimum load for the fundamental frequency, Z_1, normalized to the corresponding Class A optimum load, as a function of the conduction angle, α.

The fundamental component of the RF output power is approximately constant between the Class A and Class B operation whereas it starts to drop, considerably, for Class C operation. However, the efficiency increases as α decreases, so a trade-off between efficiency and output power must be achieved. The optimum load resistance is almost constant between Class A and Class B modes but it starts to grow towards Class C operation.

Of course, below the Class A level a larger swing into the output current is required to reach the maximum capabilities of the active device, so the input signal has to be considerably larger in order to drive the transistor appropriately. Linearity is also an issue to take into account, since the Class A mode is the only one in which the output signal is a true representation of what was inputed.

5.2.2 Harmonic Tuned or Class J power amplifier

In the classic approach, a truncated sinusoid is considered as the output current waveform and a sinusoid is chosen as the output voltage waveform. As seen in the previous subsection, to do that, the load at higher harmonic frequencies are assumed to be short-circuited, whereas the fundamental frequency requires a resistive load.

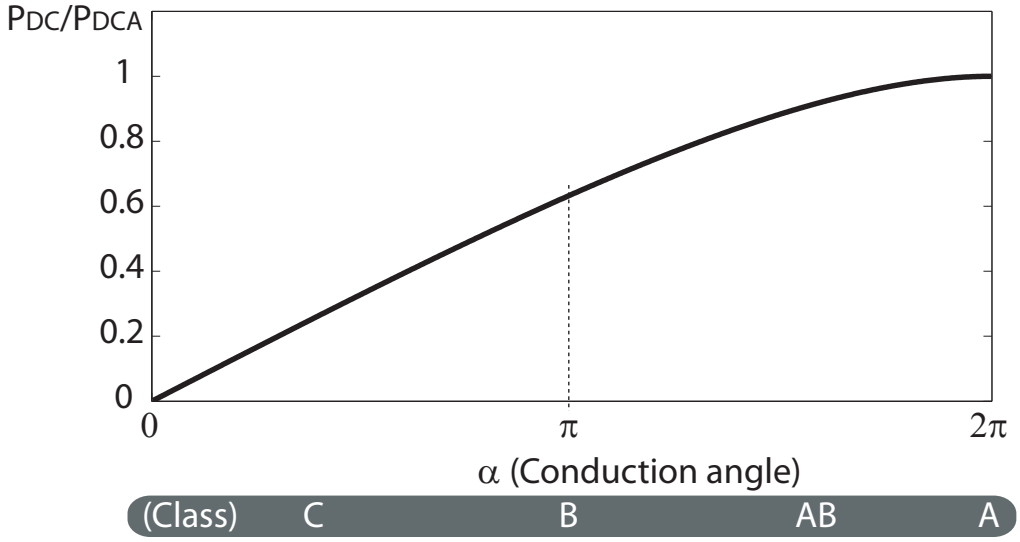


Figure 5.4: DC power, P_{DC}, normalized to the corresponding Class A DC power consumption, as a function of the conduction angle, α.

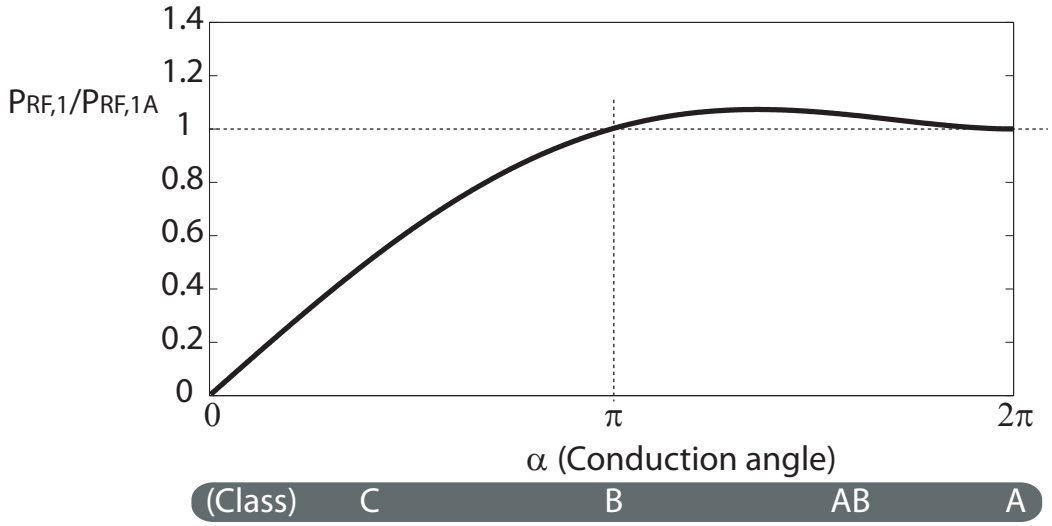


Figure 5.5: Output RF power at the fundamental frequency, $P_{RF,1}$, normalized to the corresponding Class A output RF power, as a function of the conduction angle, α.

But in practice, the design of the load at higher harmonics play a main role in the power and efficiency performance of the amplifier.

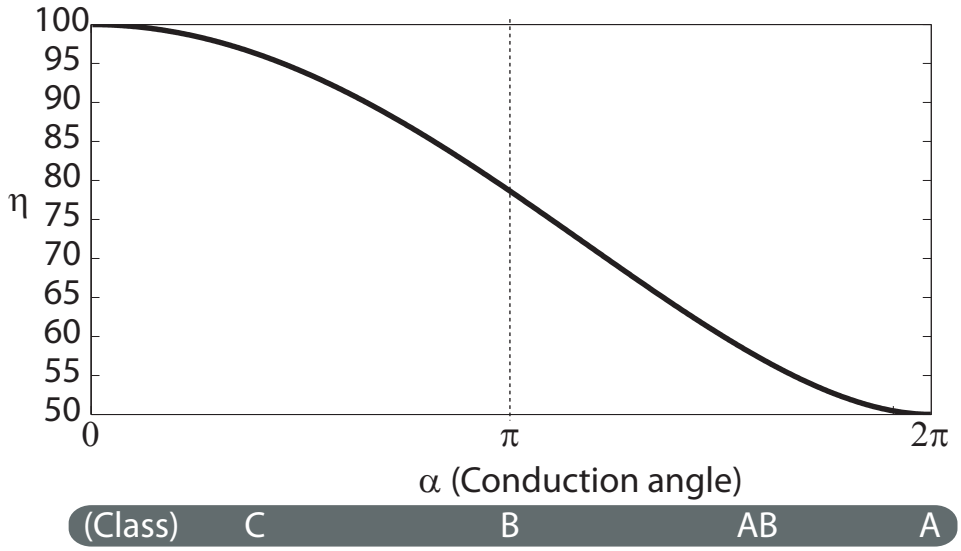


Figure 5.6: Drain efficiency, η, normalized to the corresponding Class A drain efficiency, as a function of the conduction angle, α.

This approach is usually applied to the Class AB Mode, using a particular harmonic termination. It is also known as the *Class J* [47] or simply Harmonic Tuned power amplifier [46]. The main idea is to find the "sweet spots" in a particular active device, in order to reduce the spectral distortion products almost into null over restricted power drive levels. To do so, harmonic components may not be short-circuited, as in the conventional modes, but will be properly selected, achieving different types of output waveforms. Since it is complicated to predict which kind of output waveforms will adapt better to a particular active device, the process is usually done inversely by carrying out a load-pull characterization.

The load-pull characterization is a process in which the active device is systematically set with a varying impedance for one or more harmonic components. The impedance is usually a complex value and if there are no stability issues the whole Smith chart is covered. An important advantage of this process is the possibility of representing the power and efficiency performance of the active device as contours in the Smith Chart (Fig. 5.7). The visual representation of these parameters for the different harmonics allows the achievement of a fair compromise between power and efficiency performance for a particular frequency of interest. In the example in Fig.

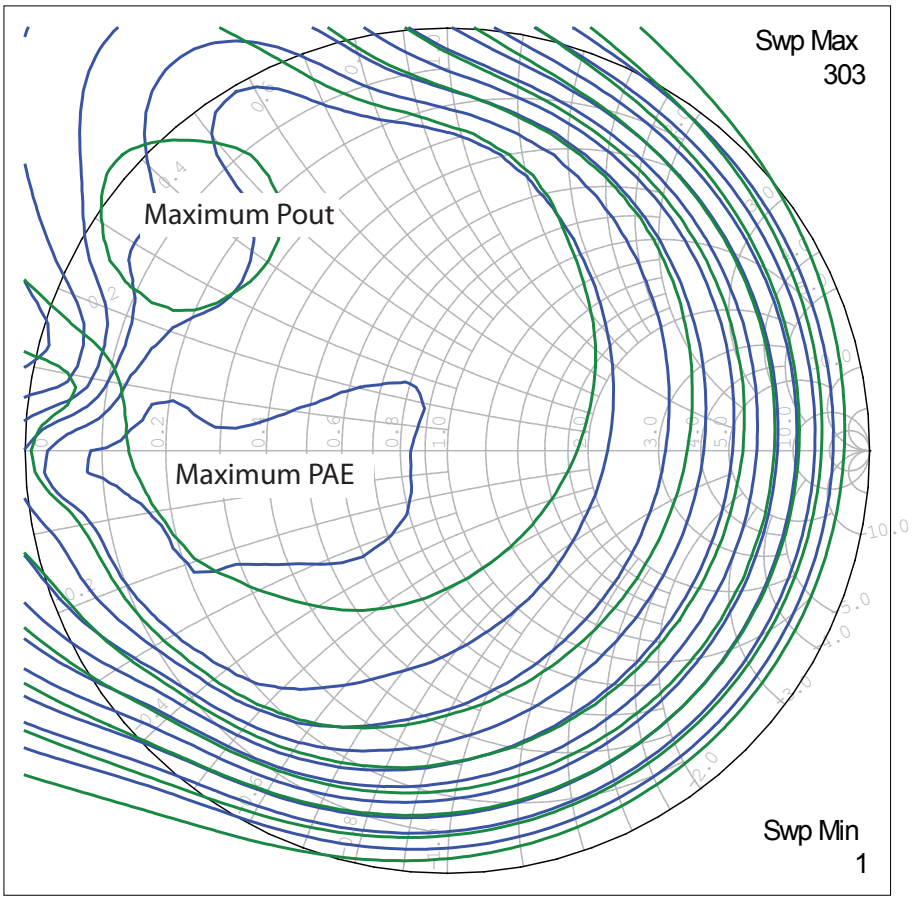


Figure 5.7: Simulated load pull output power and efficiency contours for a GaN HEMT (Cree, CGH35015F) at the fundamental load of 900MHz.

5.7, for instance, the contours for maximum output power and efficiency are not coincident, so the load impedance will be chosen depending on design requirements.

A Harmonic Tuned power amplifier design can restore the power and efficiency values close to, or even greater than the ideal classic values of a B or AB mode. The fundamental load will usually have a reactive component and the voltage and current waveforms will be far from the classic rectified sinewave. A design, manufacture and measure example can be found in Appedix C.1.

5.2.3 The Class F mode

There are many situations in which it may be interesting to trade linearity, especially amplitude linearity, for efficiency and RF output power. There is a wide range of modulation systems that can tolerate high levels of amplitude distortion, especially constant envelope systems such as GMSK or the Galileo's AltBOC modulation scheme. The sinusoidal output voltage will be replaced with a flatter, squarer periodic waveform.

In this kind of amplifier, the drain current flows when the drain-to-source voltage is flat and low, and the drain-to-source voltage is high when the drain current is zero. Hence, the product of the drain current and the drain-to-source voltage is low, as the DC power consumption is very small, which is why the efficiency increases.

To shape the drain-to-source voltage in this manner the harmonics must be set properly. There are two types of Class F RF power amplifiers [48]: odd harmonic Class F power amplifiers or simply Class F amplifiers, and even harmonic Class F power amplifiers, also known as Class F^{-1} power amplifiers (Fig. 5.8).

The output waveforms of the former, the Class F amplifier, are given by [47]:

$$i_D(\theta) = \begin{cases} I_{max} \cdot \cos\theta & \text{if} -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 0 & \text{otherwise} \end{cases} \tag{5.15}$$

$$v_{DS}(\theta) = \begin{cases} 0 & \text{if} -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 2 \cdot V_{DD} & \text{otherwise} \end{cases} \tag{5.16}$$

If these expressions are expanded into their Fourier series components according to eqs. (5.4) and (5.5), the current and voltage coefficients, I_n and V_n, are given by [47]:

$$I_n = \begin{cases} \frac{I_{max}}{\pi} & n = 0 \\ \frac{I_{max}}{2} & n = 1 \\ \frac{2 \cdot I_{max}}{\pi} \frac{(-1)^{\frac{n}{2}+1}}{n^2-1} & n \quad \text{even} \\ 0 \quad n \quad \text{odd} \end{cases} \tag{5.17}$$

$$V_n = \begin{cases} \frac{V_{max}}{2} & n = 0 \\ -\frac{2 \cdot V_{max}}{\pi} & n = 1 \\ 0 & n \quad \text{even} \\ \frac{2 \cdot V_{max}}{\pi} \frac{(-1)^{\frac{n+1}{2}}}{n} & n \quad \text{odd} \end{cases} \tag{5.18}$$

The output voltage contains only odd harmonics, shaping a perfect square waveform, and the drain current contains only even harmonics, in order to shape a truncated half-sine waveform. Current and voltage Fourier components with the same order n are alternately not present, therefore, the power delivered at harmonic frequencies is zeroed. The output network terminations, Z_n, are simply obtained as the ratio between the V_n and the I_n coefficients. Hence, the terminating impedance at the fundamental frequency must be purely resistive, an open circuit must be imposed at odd harmonics and a short circuit at even harmonics.

$$Z_n = -\frac{V_n}{I_n} = \begin{cases} \frac{4}{\pi} \cdot \frac{V_{max}}{I_{max}} & n = 1 \\ 0 & n \quad \text{even} \\ \infty & n \quad \text{odd} \end{cases} \tag{5.19}$$

The output waveforms of the latter, the Class F^{-1}, on the other hand are given by:

$$i_D(\theta) = \begin{cases} I_{max} & \text{if} -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 0 & \text{otherwise} \end{cases} \tag{5.20}$$

$$v_{DS}(\theta) = \begin{cases} 0 & \text{if} -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ -V_{max} \cdot \cos(\theta) & \text{otherwise} \end{cases} \tag{5.21}$$

Using (5.4) and (5.5) to expand them into its Fourier series components gives their expansion coefficients:

$$I_n = \begin{cases} \frac{I_{max}}{2} & n = 0 \\ \frac{2 \cdot I_{max}}{\pi} & n = 1 \\ 0 & n \quad \text{even} \\ \frac{-2 \cdot I_{max}}{n\pi} (-1)^{\frac{n+1}{2}} & n \quad \text{odd} \end{cases} \tag{5.22}$$

$$V_n = \begin{cases} \frac{V_{max}}{\pi} & n = 0 \\ -\frac{V_{max}}{2} & n = 1 \\ \frac{2 \cdot V_{max}}{\pi \cdot (n^2-1)} (-1)^{\frac{n}{2}+1} & n \quad \text{even} \\ 0 & n \quad \text{odd} \end{cases} \tag{5.23}$$

In this case, the output voltage contains only even harmonics, shaping a half-sine waveform, and the drain current contains only odd harmonics, thus creating a square current waveform. By calculating the ratio between the Fourier coefficients V_n and I_n is easy to infer that the terminating impedances, Z_n, for this configuration must be a purely resistive impedance for the fundamental frequency, a short circuit at odd harmonics and an open circuit at even harmonics.

$$Z_n = -\frac{V_n}{I_n} = \begin{cases} \frac{\pi}{4} \cdot \frac{V_{max}}{I_{max}} & n = 1 \\ \infty & n \quad \text{even} \\ 0 & n \quad \text{odd} \end{cases} \tag{5.24}$$

DC biasing is selected to eliminate the device power consumed during switching, obtaining a theoretical 100% efficiency. To do so the quiescent point must be close to the cutoff region in order to generate significant amount of harmonics. The biasing point is located slightly above the Class B operation (see Fig.5.1 (c)). Therefore, the load line and the output waveforms are similar to those of Class B. That is why Class F amplifiers are also known as overdriven Class B amplifiers. In fact, by comparing equations (5.19) and (5.24) to (5.10) it can be inferred that the terminating impedance at the fundamental frequency for a Class F amplifier is $4/\pi$ times higher than the optimum impedance obtained for the Class B operation or, $\pi/4$ times lower for a Class F^{-1}.

In practice, the number of harmonics that can be shaped are finite. In this case, the output waveform shape will be determined by the harmonic coefficients, V_n and I_n. Usually, two different approaches are taken: power amplifiers with maximally flat drain-to-source voltage and power amplifiers with maximum drain efficiency (Fig. 5.9). In general, a perfect square waveform is not achievable and an overlapping area between the drain-to-source voltage and the drain current appears dropping the efficiency below the theoretical 100%.

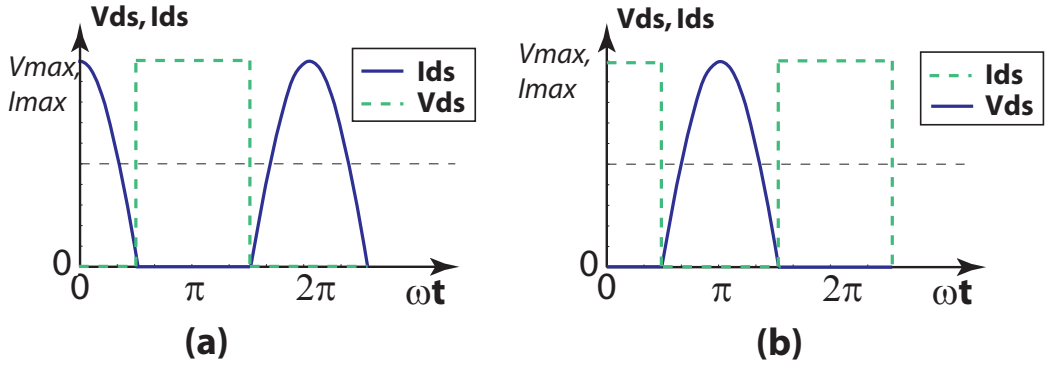


Figure 5.8: Drain voltage and drain current waveforms for a infinite order Class F (a) and a Class F^{-1} (b) power amplifier

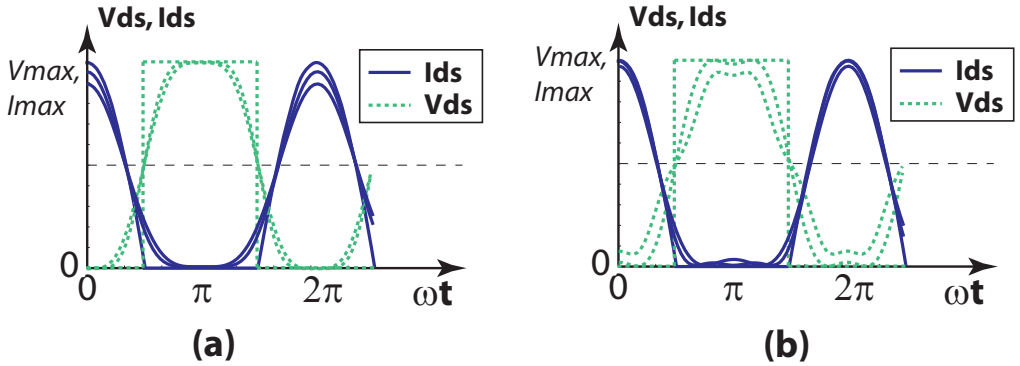


Figure 5.9: Drain voltage and drain current waveforms for a finite order Class F power amplifier with maximally flat drain-to-source voltage and a finite order Class F power amplifier with maximum drain efficiency compared to an infinite order Class F

5.2.4 The Class E mode

Class E power amplifiers are considered, along with Class F amplifiers, as switched amplifiers. These kinds of amplifiers act like a switch operating between two stages, "ON/OFF". Output voltage and current waveforms are shaped so as to prevent overlapping between them, thus minimizing power dissipation and ensuring the highest efficiency level, theoretically a 100%.

Unlike the approach used in the analysis of the Class F power amplifier, where the active device is considered to be a voltage controlled current source and the

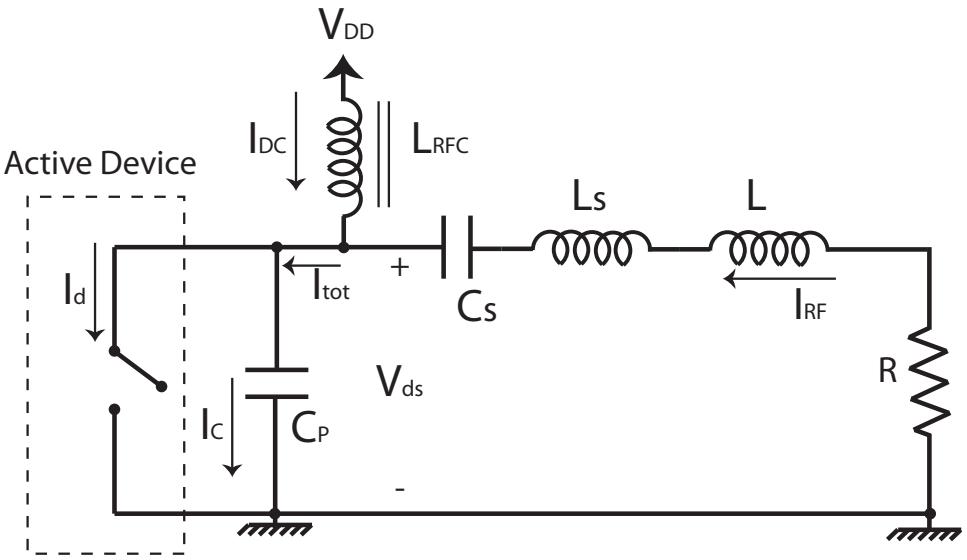


Figure 5.10: Circuit topology for a Class E power amplifier

waveform shaping is produced due to the multi-harmonic control, the Class E power amplifier is based on the hypothesis that the active device is operated as a switch. Hence, the validity of this strategy is limited to a frequency range where the effect of device parasitics is negligible and the device can be considered to work as a switch, typically moderately high frequencies, including the low microwave range.

The circuit topology of a Class E PA is shown in Fig. 5.10. In this kind of amplifier the total current, $I_{tot}(t)$, flows in the switch for the ON state, otherwise it flows in the capacitor, C_P, when the switch is OFF. On the other hand, the drain-to-source voltage, $v_{DS}(t)$ becomes and remains zero during the ON state, while its behaviour during the OFF state can be inferred by integrating the current flowing through the capacitor C_P. The device output capacitance, C_{ds}, will be absorbed into the C_P capacitance in the aforementioned topology. Usually, at high frequencies, when the output capacitance value grows no external capacitance is required.

To guarantee this behaviour, the following conditions must be fulfilled:

- The Zero Voltage Switching, ZVS condition: there must be zero voltage when the switch is ON.

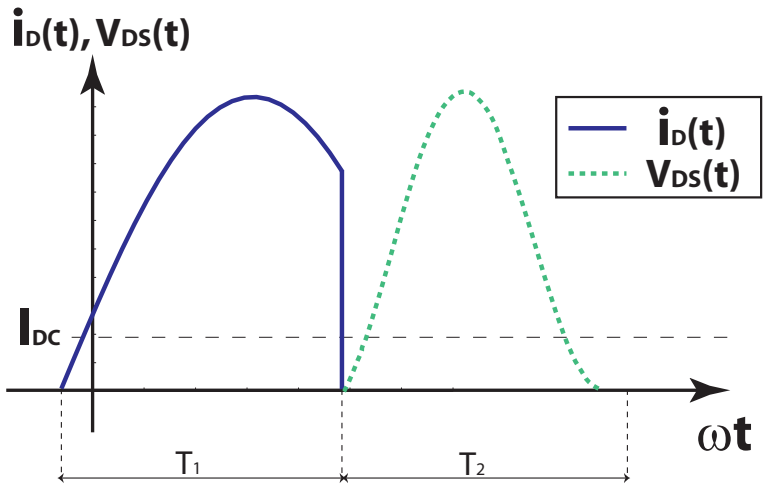


Figure 5.11: Ideal normalized Class E output current and voltage waveforms

- The Zero Voltage Derivative Switching, ZVDS condition: there must be no overlap between the voltage and current waveforms so that no loss occurs during switching.

The ideal output current and voltage waveforms are shown in Fig. 5.11 for a 50% duty-cycle (time interval for the ON/OFF states, T_1 and T_2). There is no overlap between them, so no active power is consumed during the RF operation.

The analysis of the load value and the output waveforms can be done in the time or frequency domain. When dealing with high frequency applications, the frequency domain analysis is the most practical one. It is possible to evaluate the switch loading impedance, Z_n, resulting in [47]

$$Z_{L,ext} = \frac{0.280 \cdot e^{j49.05^o}}{\omega \cdot C_P} \tag{5.25}$$

for the load at the fundamental frequency at the extrinsic plane (the one loading the switch and C_{ds}), and [47]

$$Z_{L,int} = \frac{0.346 \cdot e^{j35.94^o}}{\omega \cdot C_P} \tag{5.26}$$

for the intrinsic one (the impedance loading the switch only after embedding C_{ds}). The switching loading impedance for the harmonics are open circuit load conditions.

The quiescent point must be selected to fulfill this condition [47]:

$$I_{DC} \leq 0.349 \cdot I_{Max} \tag{5.27}$$

where I_{Max} is the maximum output current of the active device. The bias point is usually close to the cut-off region. An example of a load line for a Class E power amplifier is shown in Fig. 5.12, for this mode of operation the fundamental load line corresponds to a complex value. The transition from the ON to the OFF region and from the OFF to the ON region are also highlighted.

Nothing has been said about the choice of the input network. The only condition imposed to the input network is to drive the active device properly to operate as an ideal switch as much as possible. So, the optimum input signal would be a square waveform. That is why it is quite common to introduce a Class F stage before a Class E power amplifier. A design, manufacture and measure example can be found in Appedix C.2.

5.3 Distributed power amplifiers working at high efficiency modes of operation

The large-signal performance of any active device is determined not only by its corresponding load impedance at the operation frequency, but also, by the impedance values seen at the different frequency harmonics. As discussed in section 5.2, these are the fundamentals for high-efficiency power amplifier design.

The design of distributed amplifiers, on the other hand, is based on the synthesis of artificial transmission lines. This process determines both the fundamental and the frequency harmonics impedances. To evaluate the distributed amplifier capabilities in multi-harmonic shaping, generic expressions for the intrinsic load impedances presented at different active devices in a distributed amplifier configuration have been analyzed.

In Figs. 5.13 and 5.14, the load impedances for a 5-stage single-fed distributed

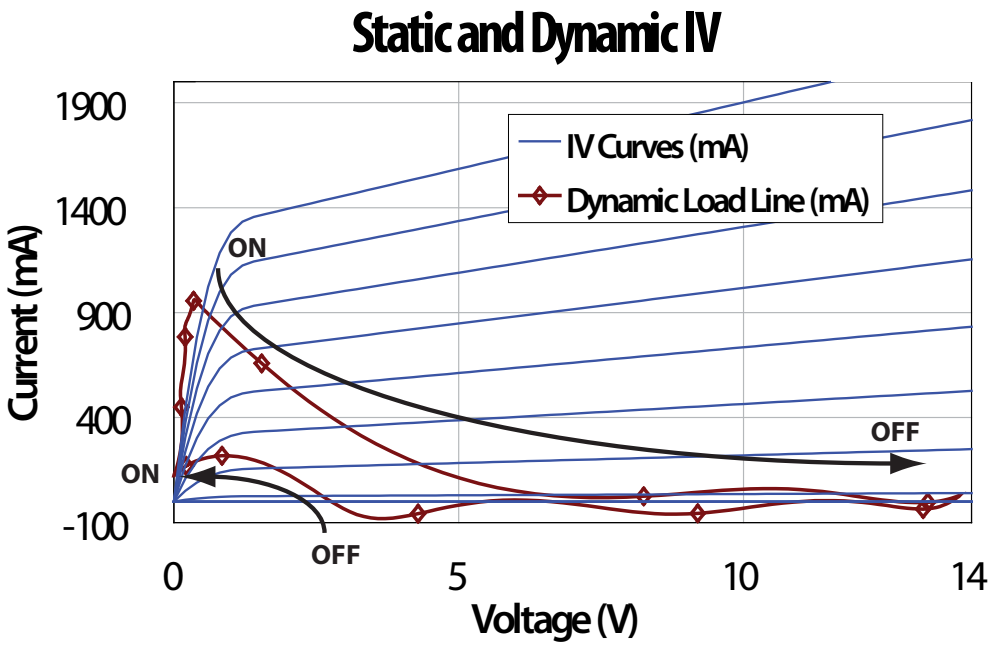


Figure 5.12: Class E amplifier load curve

amplifier using CRLH and RH-TLs are presented. It can be observed that the real part (full line) for the five active devices are frequency dependent and different during the passband, but reaches the predicted optimum value, $\frac{N}{2}Z_{0d}$ (see Chapter 2), at a discrete set of phase shift values, for instance, $\theta_g = \theta_d = 0$ or $\theta_g = \theta_d = \pi$. For these phase shifts, the real part of the load impedances of the 5 active devices are coincident and there is no imaginary part. Beyond the cutoff frequencies, however, the load impedances are fully imaginary (dashed lines). It can be observed that the behaviour of these load impedances is mainly governed by frequency response of the image impedance with π-topology (Figs. 5.15 and 5.16). The load impedance is close to an open circuit next to the cut-off frequencies and tends to a short circuit for the higher harmonics.

Design options. In Fig. 5.13 we will focus again on discussing the design possibilities associated to a distributed amplifier working as a power amplifier. In section 5.2, the classic approaches for high-efficiency power amplifier design were reviewed. The validity of such approaches in a distributed amplifier configuration will be dis-

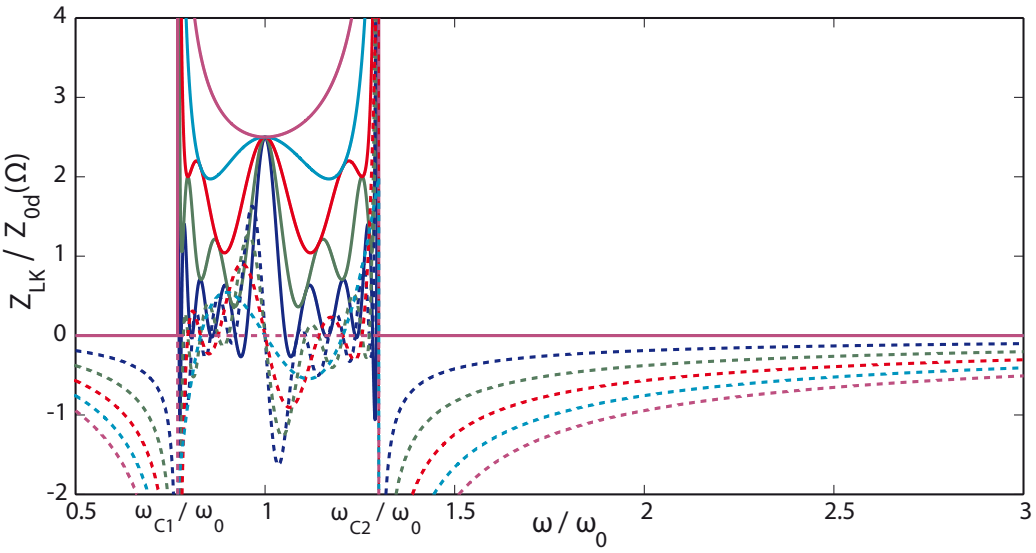


Figure 5.13: Load impedances for a 5-stage CRLH-TL-based single-fed distributed amplifier as as function of the normalized frequency (real part in full line and imaginary part in dashed line)

cussed.

1. *Class E configuration:* for the active device to work as a switch, the zero voltage and the zero voltage derivative switching conditions must be fulfilled. The analysis of the load at the fundamental frequency imposing those two restrictions gives eq. (5.26) as the load for the intrinsic plane. The evaluation of that expression tells us that, generally, the load at the fundamental frequency in the intrinsic plane of the active device will be a complex value. To achieve an identical contribution of the active devices to the output power the load impedance at the fundamental frequency must be the same for all the active devices. It has already been demonstrated that this phenomenon only appears at singular frequencies and imposes a real impedance for all the active devices. Therefore, the Class E configuration is not a suitable option to be implemented in a distributed amplifier configuration.

2. *Class F configuration:* the Class F configuration requires a real impedance at the fundamental frequency and a proper harmonic control to achieve a

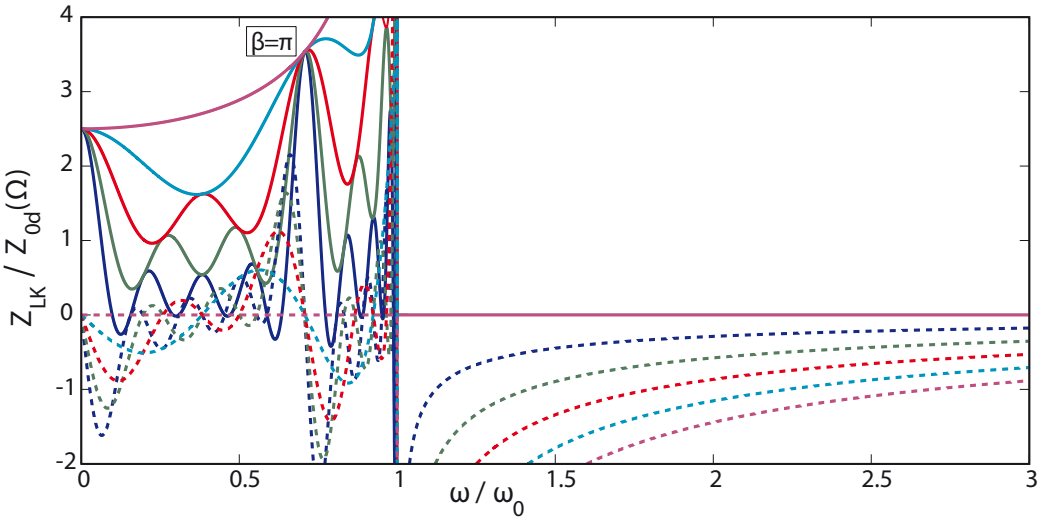


Figure 5.14: Load impedances for a 5-stage RH-TL-based single-fed distributed amplifier as function of the normalized frequency (real part in full line and imaginary part in dashed line)

square wave shaping at the output voltage/current. The first condition can be satisfied in a distributed amplifier as seen in Chapter 2, guaranteeing an identical power contribution from all the active devices. The multi-harmonic shaping is, on the other hand, a more difficult issue. The ideal Class F power amplifier requires the synthesis of an open circuit at the odd harmonics and a short circuit at the even harmonics (Class F), or the synthesis of a short circuit at the odd and an open circuit at the even harmonics (Class F^{-1}). Turning to Fig. 5.13 it is clear that the most logical strategy is the synthesis of a finite order Class F^{-1} power amplifier, since the natural behaviour of the image impedance with π-topology (Fig. 5.15) imposes an open circuit at the top cut-off frequency and tends toward a short circuit at high frequency.

However, if the load impedance in the drain line is a constant real value, e.g. 50Ω, the load impedances at the intrinsic planes in the active devices takes the form as shown in Fig. 5.17. It can be appreciated in this figure that an open circuit is not reached. To solve this problem, other authors [30] have used a multi-harmonic matching network at the output port, achieving a measured drain dc efficiency of 71%.

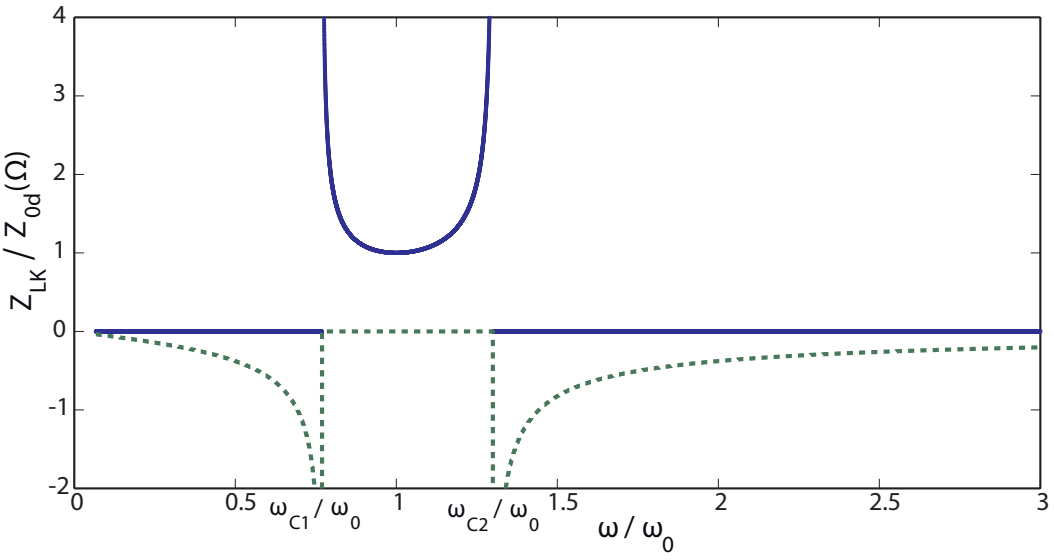


Figure 5.15: Image impedance of the drain unit cell (CRLH-TLs) with π-topology

3. *Conventional high efficiency modes:* the classic design seeks to shape a pure sinusoid as the output voltage waveform. To do so, the impedance at the fundamental frequency must be a resistive value whilst the harmonics should be short-circuited. Any classic mode of operation is suitable for this topology, for instance, Class A, AB, B or C. Surely, appropriate bias conditions and a proper design of the artificial transmission lines subject to the characteristics of the active device under these bias conditions is mandatory [29]. Since the load impedances for the active devices tends toward a short circuit if the frequency is sufficiently far from the band pass (Fig. 5.13), in order to achieve short-circuit conditions, the cut-off frequencies of the structure will have to be conveniently chosen for it to appear well before the second harmonic.

   To illustrate the theory, three different simulations in Classes A, AB and B have been performed using a Curtice cubic nonlinear FET model. A narrow band pass has been selected, so the cut-off frequency is close to the fundamental frequency and the harmonics can be considered to be short-circuited (Fig. 5.17). Figs. 5.18 , 5.19 and 5.20 shows the output waveforms and the power-added efficiency for a 3-stage CRLH-TL-based distributed amplifier working at Class A, AB and B, respectively. Fig. 5.21 shows the load impedances for the

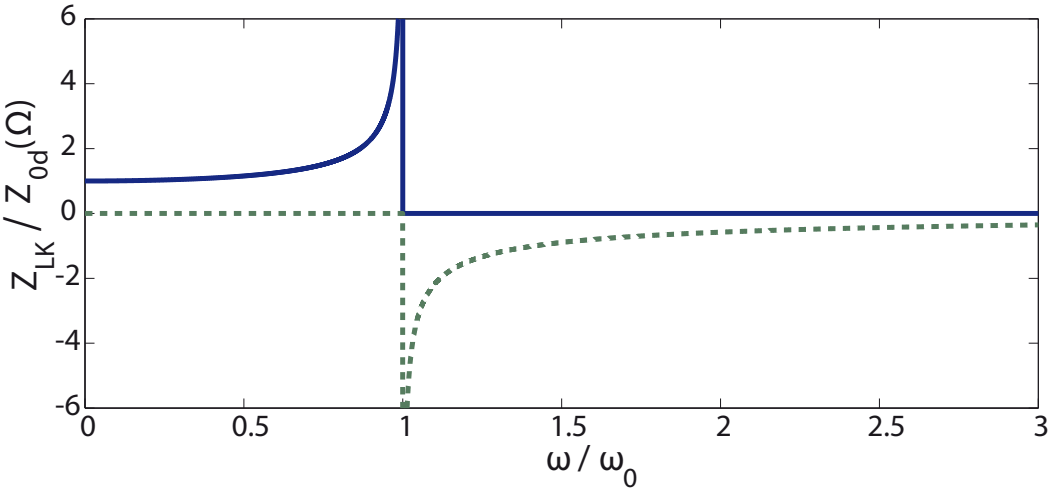


Figure 5.16: Image impedance of the drain unit cell (RH-TLs) with π-topology

three active devices working in Class A, AB, and C. The artificial transmission lines have been designed to exhibit a zero phase shift at the fundamental frequency, f_0. It can be observed from these figures that the output waveforms and the power added efficiency are close to the ideal approach (Fig. 5.1). Furthermore, at f_0, the phase shift between stages has been chosen to be zero, so the load lines and the output waveforms are identical for the three active devices. Therefore, by making a proper selection of the active device's bias point and a suitable design of the artificial transmission lines, it is possible to design an optimum Class A, AB, B or C output power combiner.

5.4 Class AB distributed power amplifier design example

In this section, a more realistic simulation of a Class AB distributed power amplifier design has been assessed. For this reason, a GaN HEMT Die with 8W output power, the CGH60008D (see Fig. 5.22) has been selected. The large signal model provided by the manufacturer, Cree, has been used and a 3-stage CRLH-TL-based distributed amplifier has been designed for the centre frequency of 2.4GHz. Phase shifts for the artificial transmission lines have been set to zero at the centre frequency for both

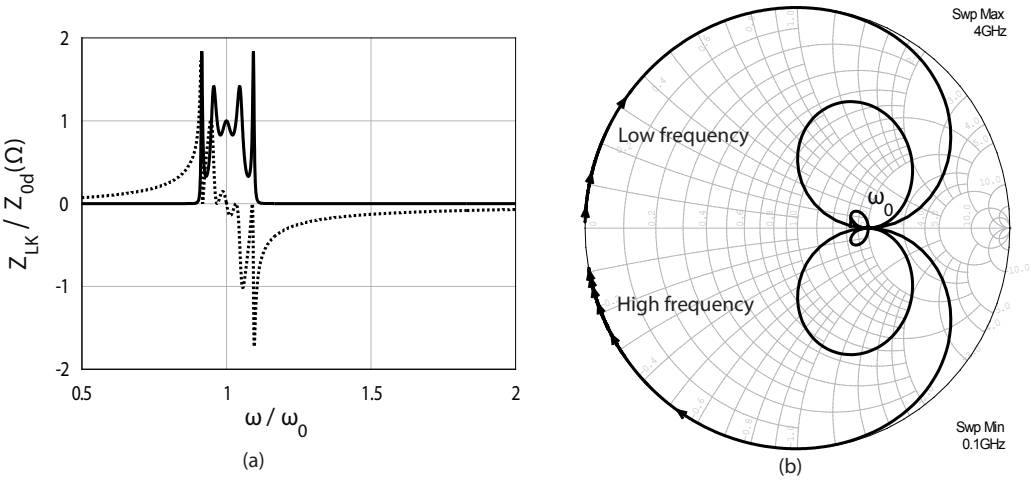


Figure 5.17: (a) Load impedance CRLH-TL-based single-fed distributed amplifier as function of the normalized frequency (real part in full line and imaginary part in dashed line). (b) Load impedance representation in the Smith Chart.

the gate and the drain lines.

A 75Ω characteristic impedance has been chosen for the drain line, in order to set the optimum load impedances, 112Ω, for all the active devices. The characteristic impedance of the gate line has been set to 50Ω for measurement purposes. The bias point, corresponding to a class-AB mode, has been set to $V_{gs} = -2.7V$ and $V_{ds} = 40V$. Ideal CRLH artificial transmission lines have been designed (see Fig. 4.6), and the selected component values are listed in table 5.2. The cut-off frequencies have been selected for it to appear well before the second harmonic, being $f_{c1d} = 2.2GHz$, $f_{c2d} = 2.6GHz$, $f_{c1g} = 2.08GHz$ and $f_{c2g} = 2.72GHz$.

Table 5.2: CRLH-TLs ideal components

C_{R_g}	$C_{R_{gaux}}$	L_{R_g}	C_{L_g}	L_{L_g}
10pF	7.5pF	25nH	0.18pF	0.44nH
C_{R_d}	$C_{R_{daux}}$	L_{R_d}	C_{L_d}	L_{L_d}
9.6pF	9pF	54nH	0.08pF	0.46nH

The simulated S-parameters are shown in Fig. 5.23 from 2.2 to 2.6 GHz. The figure shows the forward and reverse gains of the distributed amplifier and the

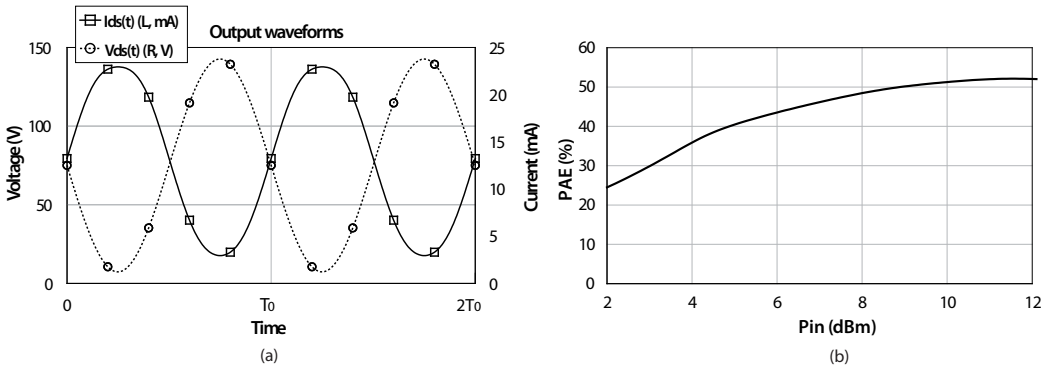


Figure 5.18: Theoretical output waveforms (a) and power added efficiency (b) for a Class A distributed power amplifier @ f_0 ($I_{DS} = 79.5mA$, $V_{DS} = 12.5V$).

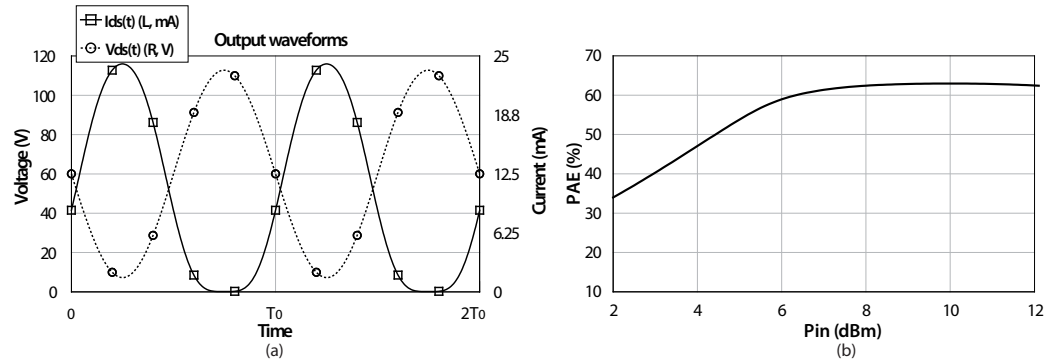


Figure 5.19: Theoretical output waveforms (a) and power added efficiency (b) for a Class AB distributed power amplifier @ f_0 ($I_{DS} = 41.5mA$, $V_{DS} = 12.5V$).

amplifier response when both outputs are combined through a Wilkinson output combiner. The gain increases by 3dB compared to the forward or reverse cases as expected. The input and output match are also assessed in this figure, showing an input match better than 10dB for the frequency of interest.

Its large signal performance has also been simulated in Figs. 5.24 to 5.28. In Fig. 5.24, the dynamic load lines for the three active devices for the P1dB are plotted. The traces are identical, which demonstrate that they are working under the same load conditions and thus delivering the same power to the output port. Fig. 5.25 shows the output current and voltage waveforms for the three active devices for the P1dB. They are those related to a Class AB mode of operation, with the maximum

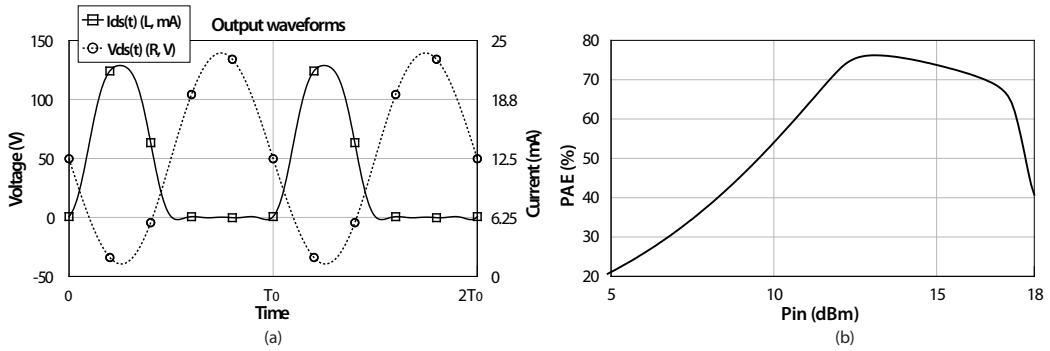


Figure 5.20: Theoretical output waveforms (a) and power added efficiency (b) for a Class B distributed power amplifier @ f_0 ($I_{DS} = 0.067mA$, $V_{DS} = 12.5V$).

sinusoidal excursion for the voltage and a truncated sinusoid for the current. This behaviour is evidenced again in Figs. 5.26 and 5.27 where the harmonic components are shown. It can be seen, as expected, that the voltage harmonic components are practically null except for the DC and the fundamental components of the output signal.

Fig. 5.28 shows the output power and the efficiency of the amplifier with output power combination and single-fed excitation. The output power reaches 42.6 dBm, which is close to the 43.7 dBm corresponding to three active devices delivering 8 W output power and the efficiency is close to 60%.

The gain performance can be further increased with the aid of the power recycling configuration (see Chapter 3), as is shown in Fig. 5.29, achieving a large signal simulation performance almost identical to a single-fed excitation.

5.5 Summary

In this chapter the theory developed in chapters 2 and 3 has been extended from Class A towards a more efficient modes of operation. To do this, a review of the fundamentals for power amplifier design has been made. The conventional high efficiency modes of operation, the harmonic tuned power amplifier, the Class F power amplifier, and the Class E mode have been detailed by analyzing the load impedances seen at different harmonics.

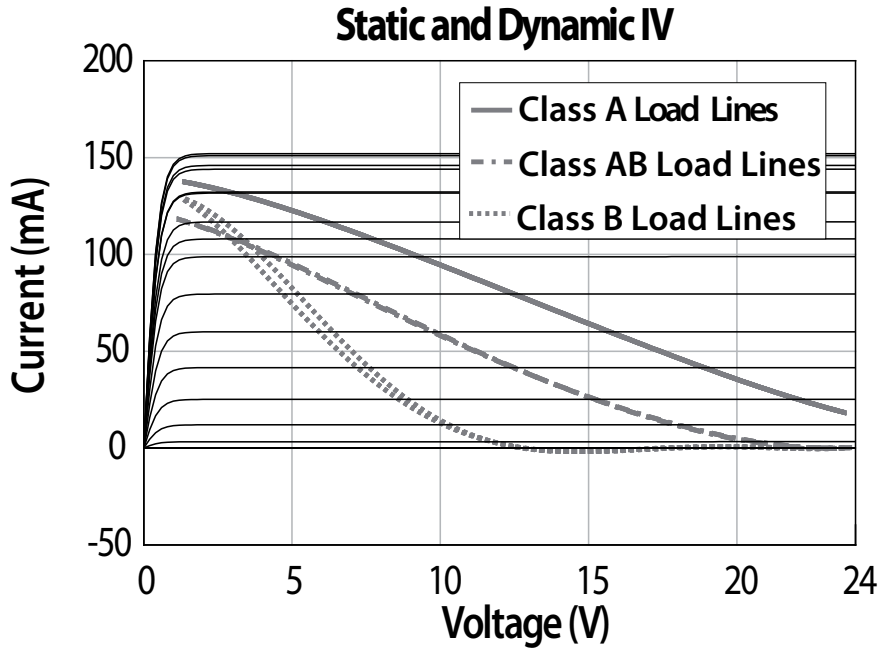


Figure 5.21: Variation of the dynamic load lines at the fundamental frequency for the active devices of a CRLH-TL-based distributed amplifier working under different modes of operation (A, AB and B).

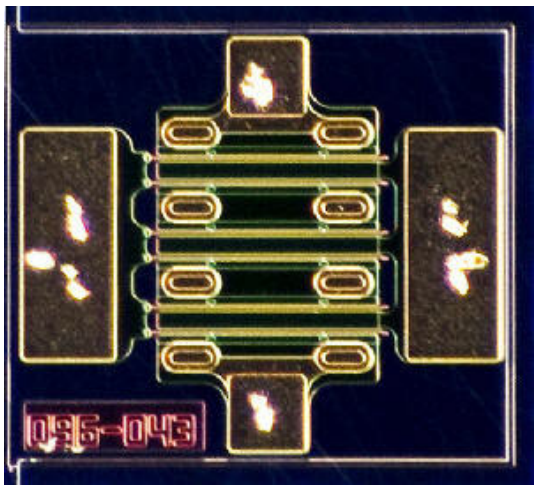


Figure 5.22: Cree's CGH60008D GaN HEMT Die

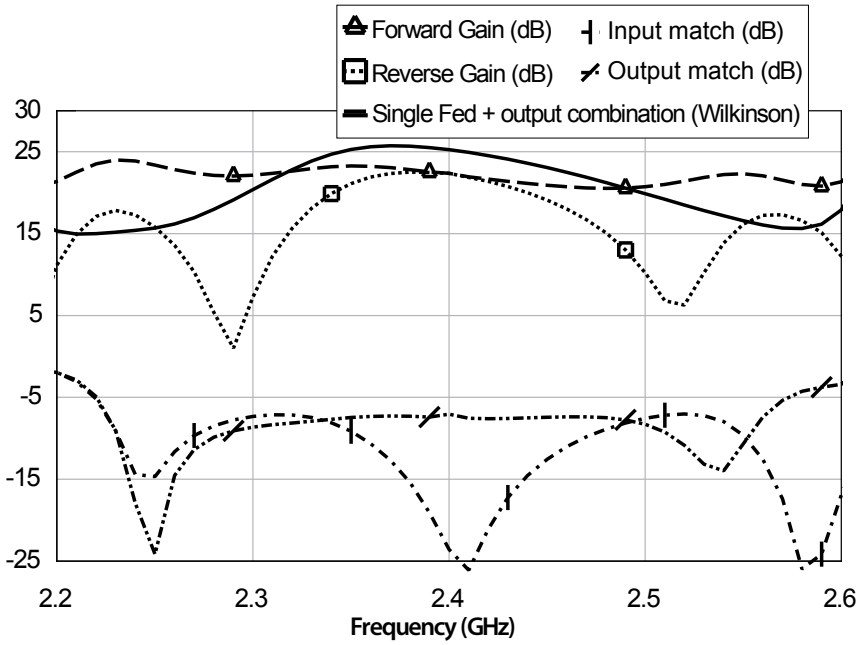


Figure 5.23: Simulated S-parameters of a 3-stage CRLH-TL-based distributed power amplifier working under Class AB

The theory was applied to the distributed amplifier design, by means of the assess of the viable configurations and their corresponding expected performance. The results show that the power recycling distributed amplifier can also work at several non-linear modes, such as Class A, AB, B, C, but cannot work at modes that require a complex load impedance at the fundamental frequency, such as Class E.

A distributed power amplifier Class AB design in power recycling configuration is proposed with a GaN HEMT active device. Simulation results prove that it is possible to design a distributed power amplifier working as an optimum power combiner and achieving, at the same time, high efficiency levels.

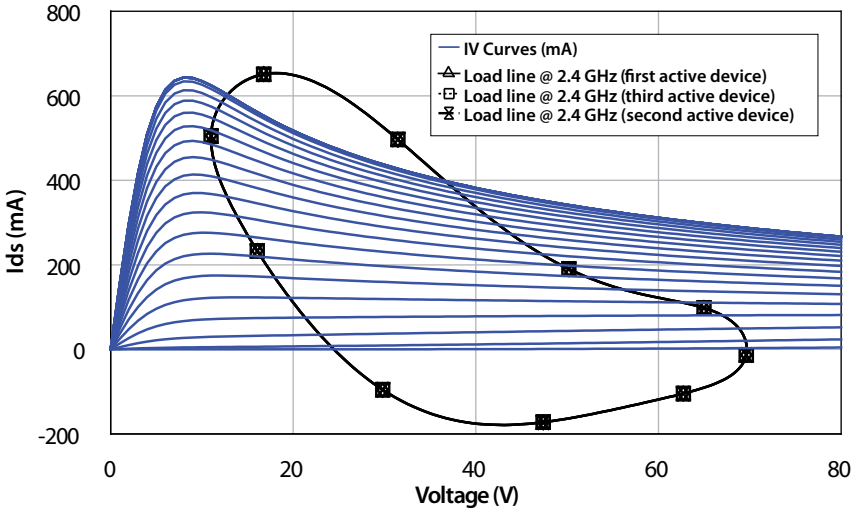


Figure 5.24: IV Curves and Dynamic load lines for a 3-stage Class AB distributed power amplifier with output power combination ($V_{GS} = [-3 : 0.2 : 2]V$, $P_{in} = 18dBm$)

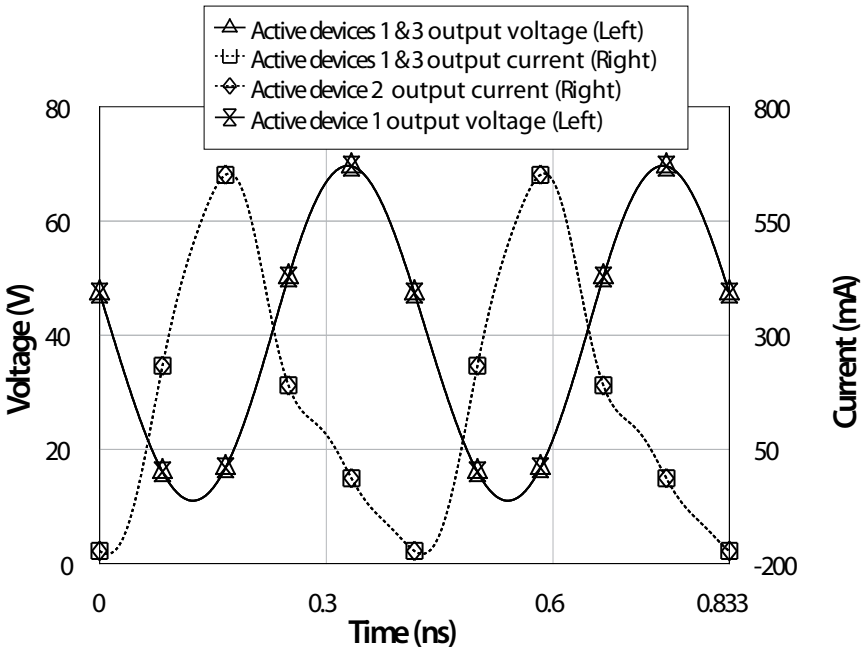


Figure 5.25: Output current and voltage waveforms for 3 active devices of a Class AB distributed power amplifier with output power combination @ f_0 ($P_{in} = 18dBm$)

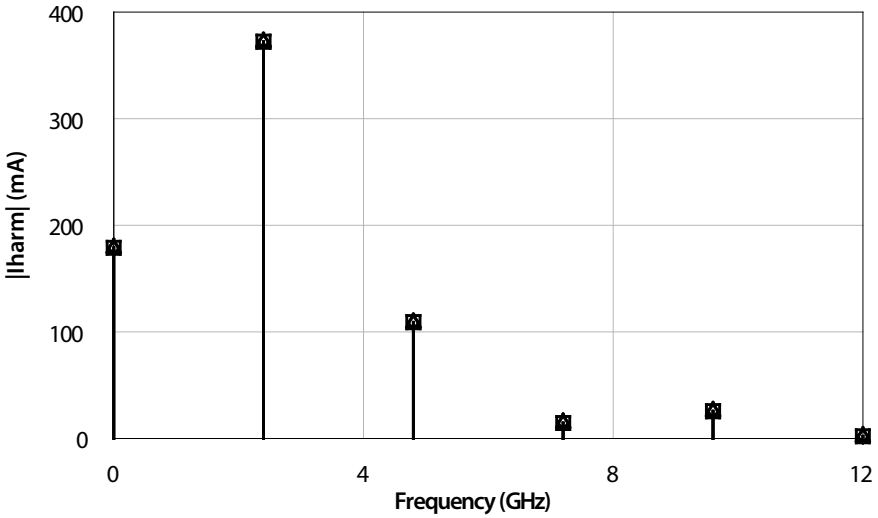


Figure 5.26: Harmonic components for the current for a 3-stage Class AB distributed power amplifier with output power combination ($P_{in} = 18dBm$)

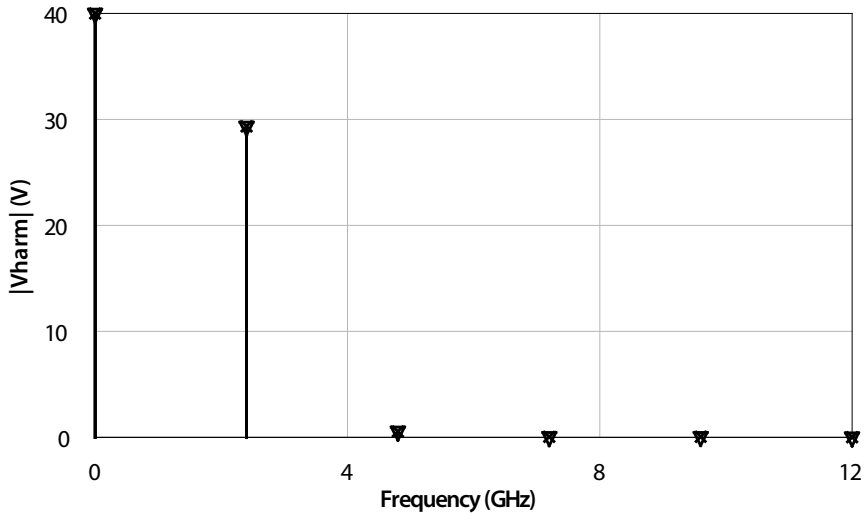


Figure 5.27: Harmonic components for the voltage for a 3-stage Class AB distributed power amplifier with output power combination ($P_{in} = 18dBm$)

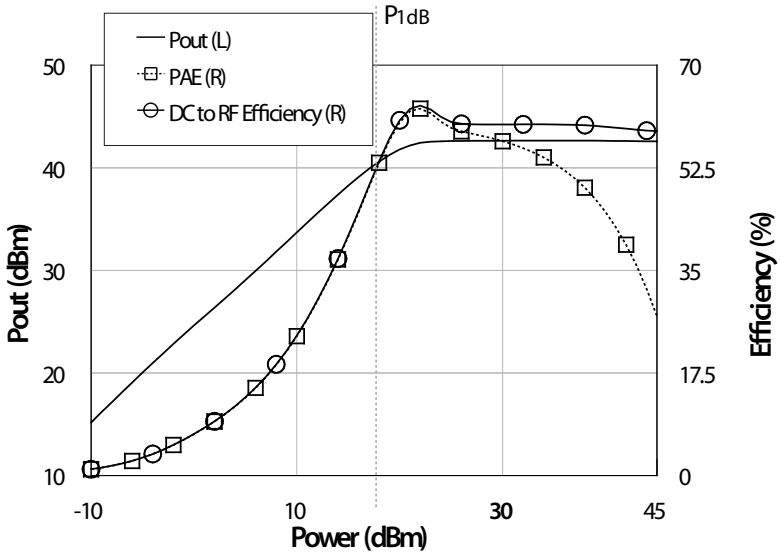


Figure 5.28: Output power and Power added efficiency of a 3-stage Class AB distributed power amplifier with output power combination

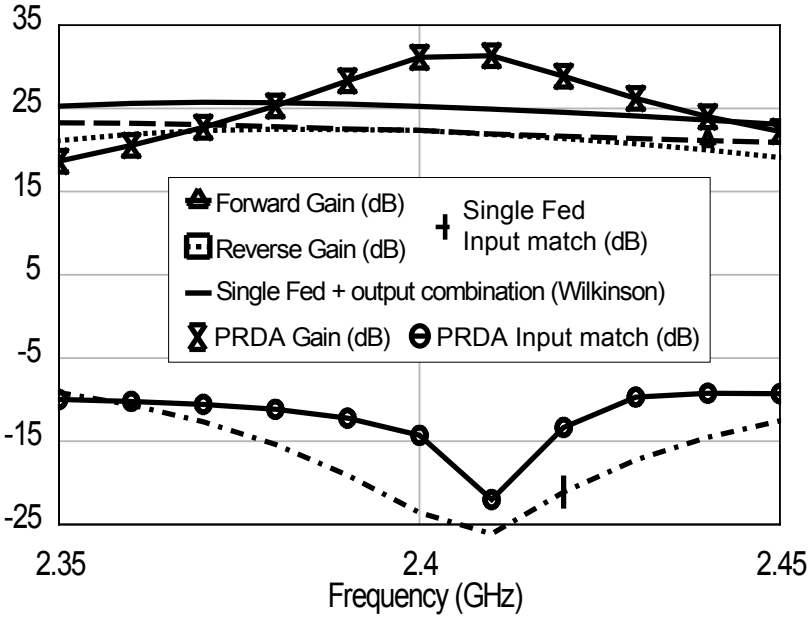


Figure 5.29: Simulated small-signal S-parameters of a 3-stage CRLH-TL-based power recycling distributed power amplifier working under Class AB

Chapter 6

Conclusions

This dissertation set out to investigate innovative ideas, inspired on metamaterials, that might add to the existing offer in matters of distributed power amplification. In this final Chapter, the research contributions of this dissertation will be reviewed, and directions for future research will be discussed.

6.1 Contributions

Chapter 2 constitutes the basis on which the rest of the work is founded. It reviews the already-known gain analysis of distributed amplifiers, in order to give a full understanding of the results to the readers, and carries out a comprehensive study of the intrinsic power performance of uniform distributed amplifiers. For that task, the load impedances of the active devices that make up a generic distribute amplifier are analyzed. This analysis can be considered as one of the major contributions to this thesis since it sets the basis for the study of such an structure as a power amplifier. The results obtained confirm that there is a discrete set of phase shifts that can be applied to the artificial transmission lines, to make all the transistors work under the same, real, load conditions. Under such conditions the distributed amplifier can thus work as an optimum class A power combiner. The analysis also reveals that the application of CRLH-TLs can be exploited to achieve bandpass behaviour and chip reduction. These results are further extended to an alternative architecture with simultaneous power injection, the so-called dual-fed distributed amplifier, with a similar outcome.

This work has also responded to a question that remained unanswered in the literature. In ***Chapter 3*** an innovative architecture is proposed and analyzed to solve the two main problems of distributed power amplification: the power wasted in the idle port and the unequal load conditions of the active devices. The Power Recycling Distributed Power Amplifier appears as an alternative to other existing distributed-based power amplifiers offering ideal perfect input match conditions, identical load conditions for the active devices, full output power combination and a gain control system determined by the input directional coupler. Due to the aforementioned characteristics, this new architecture might be of interest for high frequency applications where the available output power of the active devices is scarce and the power combination is mandatory. Furthermore, the gain enhance at such a high frequency range could be crucial to meeting the requirements of potential applications.

Experimental verification of the ideas developed in previous chapters are presented in ***Chapter 4***. For this reason, this chapter is key in this dissertation. In the chapter, the experimental results published in [16] are fully detailed. To the authors' knowledge, these results are the first ones that can be found in the literature of a power distributed amplifier prototype using CRLH unit cells designed for $\theta = 0$ at the operation frequency. The theory detailed in [16] was recently adopted by Fei et al. [41] for the implementation of a 2-D power amplifier for 60 GHz in 65 nm CMOS, thus proving the viability of a metamaterial-based distributed power amplifier design for different technological processes. Small- and large-signal measurements taken in this first prototype have confirmed the conclusions derived from the simplified intrinsic analysis of chapter 2. Gain values are consistent with theory, and output power and efficiency performance shows that the amplifier is working as a class-A power combiner. This prototype was followed by a second version of the power amplifier, targeted to verify the conclusions derived from Chapter 3. For this task a CRLH-TL-based power recycling distributed amplifier was designed. The prototype was measured in the small-signal regime to support the conclusions extracted from the analysis of the PRDA architecture. The measurements show the enhancement in the gain values and a very good input match conditions. The same prototype has been compared to the single- and dual-fed configurations confirming the superiority of the performance of the PRDA. These results confirm the viability of a distributed

power amplifier working as an optimum power combiner with the added benefit of an enhanced gain, which can be arbitrarily chosen through a proper design of the directional coupler, with an almost perfect input match conditions. The chapter continues with a distributed power amplifier design in monolithic technology. This last design has two important features: firstly, it represents the technological leap to the monolithic technology design, which is desirable to be able to work at high frequencies, and secondly, it studies the behaviour of a power distributed amplifier under complex modulation schemes. The designed amplifier, aimed at LTE applications, has been simulated under small-, large-signal and modulated signal showing good results in terms of ACPR and EVM performance.

Finally, the work presented in ***Chapter 5*** appears as the natural step of the previously conducted analysis. The chapter reviews different high efficiency modes of operation and relies on the intrinsic power analysis carried out in Chapter 2 to study the behaviour of a distributed power amplifier when different strategies are applied to harmonic shaping. The Chapter concludes that it is possible to design any of the classic modes, namely A, B, AB or C, and the inverse class F mode. However, the modes that do require a complex load at the fundamental, i.e. the class E mode, are discarded due to the intrinsic behaviour of a generic distributed amplifier. Simulations have been presented to support the theoretical results, and a Class AB distributed power amplifier design in power recycling configuration with a 8W GaN HEMT Die is presented. The results show that it is possible to design a distributed power amplifier working as an optimum power combiner with high efficiency levels and enhanced gain.

6.2 Future work

The future work related to this dissertation can be organized as follows:

1. Manufacturing of a high efficiency distributed power amplifier: this task is the natural continuation of the work presented in Chapter 5. At the end of the chapter a Class AB distributed power amplifier design was simulated. Obviously, the next step is to manufacture and measure it with a modulation scheme according to the operation frequency, which would take advantage of

the increase in the output efficiency. Of course, this type of design makes more sense when an active device with a high output power density is used, namely a GaN device. In this regard, the work described in Section 5.4 that has been carried out with an 8W GaN Cree transistor fits perfectly with future expectations.

2. Inclusion of a phase-tuning mechanism in the PRDA architecture: since the phase conditions is a key requisite for a proper design of the PRDA architecture, it is desirable to include some kind of mechanism that could serve as a fine tuning in the final phase conditions once the prototype is manufactured. The idea is to include a voltage controlled phase shifter between the input directional coupler and the 4-port distributed amplifier that would serve this purpose through an external port.

3. Analytical study of the intrinsic behaviour of non-uniform distributed power amplifiers: in this Thesis, a comprehensive study of the intrinsic behaviour of uniform distributed power amplifiers has been carried out, and the particular conditions for optimum power combination in this structure have been highlighted. It would be interesting to continue this work by carrying out an exhaustive analysis of the non-uniform distributed power amplifiers. There have been several works published over the years [10; 11; 19; 21], that have achieved good results by modifying the unit cells between stages in the drain line and the periphery of the active devices. General and closed-form expressions that might encompass these works would be desirable.

4. Frequency scaling: the last task that will be proposed is related to the potential applications for the PRDA. This new architecture will have to compete with other current topologies that have been developed with the same purpose. The key element of the PRDA resides in the gain control mechanism that can be applied through a proper design of the directional coupler combined with an almost perfect input match. As was mentioned earlier this feature could be of great interest at high frequencies were the available output power of the active devices is low, and the only way to meet the standard's requirements is through the power combination. Having an extra degree of freedom concerning

the available gain can make the difference between one architecture or another. Therefore, it is interesting and desirable to shift the design upward in frequency to achieve the full potential of such an innovative architecture. The concept has recently been validated by Fei et al. [41] for a high frequency range, through the design of a 2-D distributed power amplifier with zero phase shift for 60 GHz in 65 nm CMOS based on the theoretical concept published by the author of this Thesis in [42]. Therefore, there are good prospects for the distributed amplifier design in monolithic technology that has been presented in Section 4.3.

Appendix A

Artificial Transmission Line Theory

The parameters of a real transmission line, for instance, the phase shift, characteristic impedance, transmission time delay, and any other parameter, can be simulated through a four-terminal electrical network known as an artificial transmission line (ATL).

ATLs are implemented in different technologies, for example hybrid or monolithic technology, and can be implemented using lumped elements, or by periodically loading transmission lines.

The ideal artificial transmission line has a purely resistive characteristic impedance with negligible attenuation. To implement this network lossless components must be considered. Under such circumstances, the structure presents a filtering response with one or more cut-off frequencies. The characteristic impedance of this network is frequency dependent, being resistive in the frequency range contained within the limits of the cut-off frequencies yet at other frequencies it becomes reactive. Therefore, any signal traveling through an ATL may suffer phase delay and distortion. The behavior of an ideal ATL can be easily evaluated using the image impedance theory.

A.1 Image impedance theory

To define the image impedance, an arbitrary reciprocal two-port network, where the network is specified by its $ABCD$ parameters, will be considered. The image impedances, Z_{i1} and Z_{i2}, are defined as follows [39]:

- Z_{i1} is the input impedance at port 1 when port 2 is terminated with Z_{i2}.
- Z_{i2} is the input impedance at port 2 when port 1 is terminated with Z_{i1}.

The expressions for the image impedances can be extracted from the relationship between port voltages and currents. In terms of the $ABCD$ parameters of the network the port voltages and currents are related as [39]:

$$V_1 = AV_2 + BI_2 \tag{A.1}$$

$$I_1 = CV_2 + DI_2 \tag{A.2}$$

Obtaining the input impedance at port 1 and 2, Z_{in1} and Z_{in2}, as the relation between the voltage and the current of the corresponding port, and imposing the following conditions $Z_{in1} = Z_{i1}$ and $Z_{in2} = Z_{i2}$, Z_{i1} and Z_{i2} can be solved as follows [39]:

$$Z_{i1} = \sqrt{\frac{AB}{CD}} \tag{A.3}$$

$$Z_{i2} = \sqrt{\frac{BD}{AC}} \tag{A.4}$$

If the network is symmetric, then $A = D$ and $Z_{i1} = Z_{i2}$ as expected. The propagation constant of the two-port network can also be easily computed by obtaining the voltage transfer function of the two-port network terminated in its image impedances, where

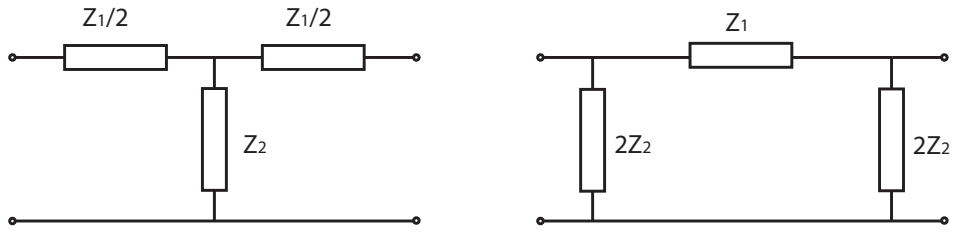
$$e^{\gamma} = \sqrt{AD} + \sqrt{BC} \tag{A.5}$$

which can also be expressed as

$$cosh\gamma = \sqrt{AD} \tag{A.6}$$

Two important types of symmetric two-port networks are the T and π networks. Their main parameters are summarized in table A.1 [39]:

Table A.1: Image Parameters for T and π Networks



T Network	**π Network**
ABCD parameters	
$A = 1 + Z_1/2Z_2$ $B = Z_1 + Z_1^2/4Z_2$ $C = 1/Z_2$ $D = 1 + Z_1/2Z_2$	$A = 1 + Z_1/2Z_2$ $B = Z_1$ $C = 1/Z_2 + Z_1/4Z_2^2$ $D = 1 + Z_1/2Z_2$
Z parameters	*Y parameters*
$Z_{11} = Z_{22} = Z_2 + Z_1/2$ $Z_{12} = Z_{21} = Z_2$	$Y_{11} = Y_{22} = 1/Z_1 + 1/2Z_2$ $Y_{12} = Y_{21} = 1/Z_1$
Image impedance	
$Z_{iT} = \sqrt{Z_1 Z_2}\sqrt{1 + Z_1/4Z_2}$	$Z_{i\pi} = \sqrt{Z_1 Z_2}/\sqrt{1 + Z_1/4Z_2} = Z_1 Z_2/Z_{iT}$
Propagation constant	
$e^{\gamma} = 1 + Z_1/2Z_2 + \sqrt{Z_1/Z_2 + Z_1^2/4Z_2^2}$	

The different two-port networks that can be implemented, considering a lossless situation, may present several pass- and stop-bands depending on their circuital topology [49], which are delimited by one or more cutoff frequencies. The propagation factor, γ, will be purely imaginary, thus allowing the signal transmission, for a pass-band and purely real, hence lossy, for a stop-band. Being a discrete structure, the phase constant is always constraint between π and $-\pi$.

Fig. A.1 presents a the circuital topology of a conventional RH unit cell with T- and π-topology. Its corresponding propagation constant is shown in Fig. A.2, and

corresponds to the conventional low pass transmission line with just one passband and one stopband. Figs.A.3 and A.4 shows the image impedance of the structure with π and T topology, respectively.

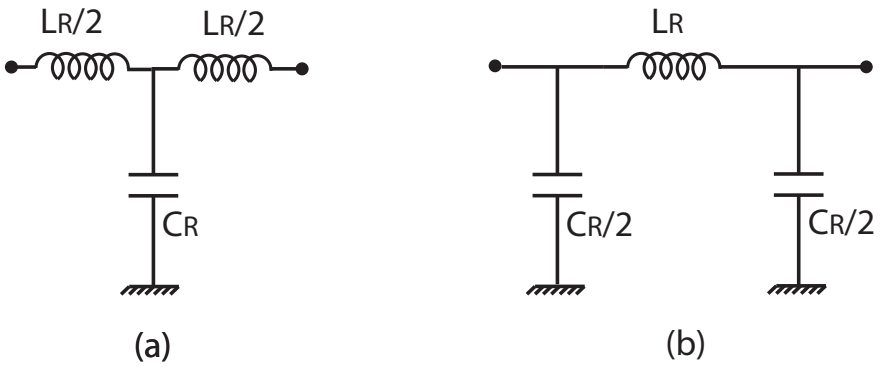


Figure A.1: Conventional RH unit cell with (a) T- and (b) π-topology

The same has been done with a CRLH unit cell with T- and π-topology (Fig. A.5). Figs. A.6, A.7 and A.8 show the propagation constant and the image impedances of this topology. In this particular case, which presents a pass band behaviour, there is a passband and a couple of stopbands.

A.2 Composite Right/Left-Handed Transmission Lines

It is not the purpose of this section to fully develop the equations that define the behaviour of this particular two-port network but to describe, in a qualitative manner, how to use the equations [24] that describe such a network during a design process.

A CRLH-TL is a two-port network, and can be viewed as a band-pass filter [24]. It can be completely analyzed by using the image impedance theory already seen in the previous section. Therefore, the image impedances and propagation factors listed in Table A.1 also apply to a CRLH-TL, being $Z1 = j(\omega L_R - \frac{1}{\omega C_L})$ and $Y2 = j(\omega C_R - \frac{1}{\omega L_L})$.

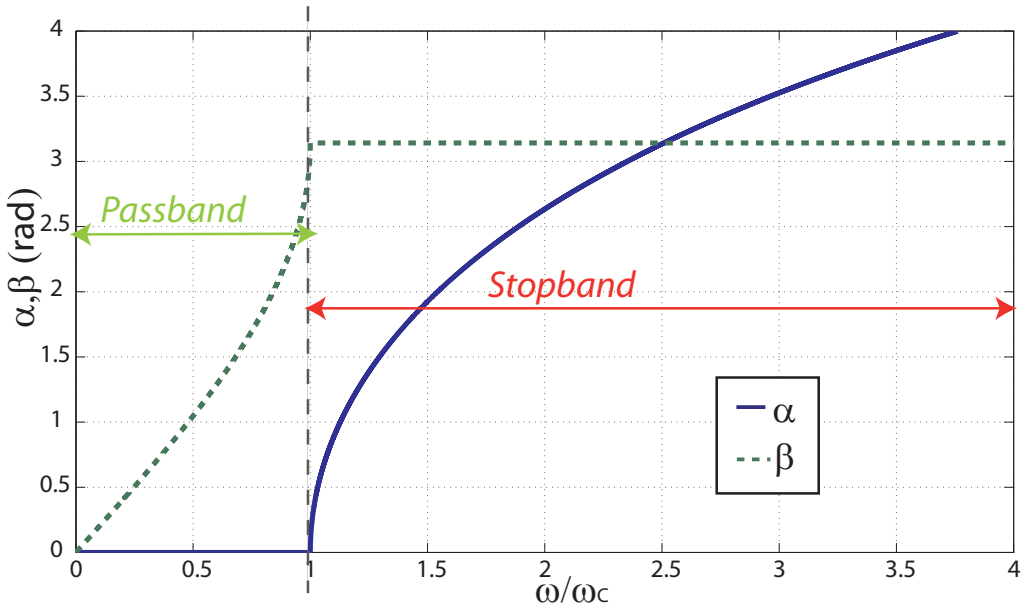


Figure A.2: Propagation constant of a conventional RH-TL unit cell

An artificial CRLH-TL has four elements: a series inductance, L_R, a shunt capacitance, C_R, a series capacitance, C_L and a shunt inductance, L_L. The first two elements are those that could be found in a purely RH TL with a positive phase constant. The other two are those that would form a purely LH TL, which would possesses a negative phase constant. A purely LH TL cannot exist physically because of the parasitic series inductance and shunt capacitance effects and therefore a CRLH is usually designed, whose dispersion diagram can be found in Fig. A.6. Please note that there are two distinguishable frequency ranges corresponding to the RH ($\beta > 0$) and LH ($\beta < 0$) behaviour.

Those four elements provide four degrees of freedom during the design process which can control several properties of the TL. The first step during the design process is to decide between a balanced, in which the series and shunt resonances are equal ($\frac{1}{\sqrt{L_R C_L}} = \frac{1}{\sqrt{L_L C_R}}$), or an unbalanced TL, in which a gap during the passband frequency range appears (Fig. A.9) as a consequence of the different series and shunt resonances. As can be appreciated in this figure a new stop-band appears in the middle of the pass-band where the signal will not be transmitted and a attenuation factor is present. If a balanced designed is selected the following relationship between

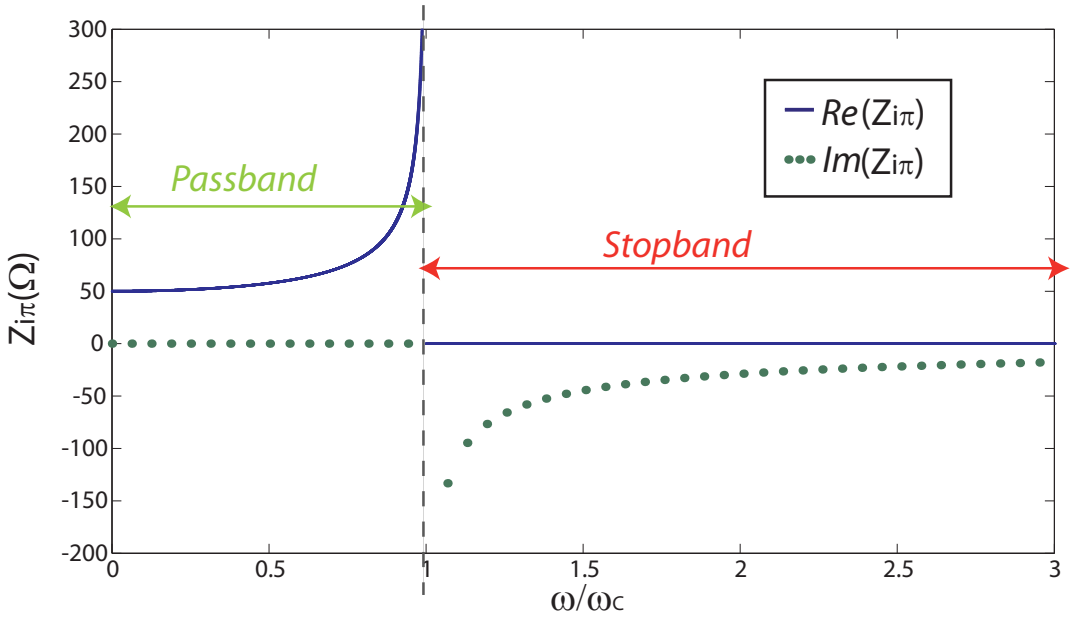


Figure A.3: Image impedance of a conventional RH-TL unit cell with π-topology

the four elements must be fulfilled:

$$L_R C_L = L_L C_R \tag{A.7}$$

The second degree of freedom can determine the $\beta = 0$ frequency or the frequency of maximum attenuation for an unbalanced unit cell, $\omega = 0$, where:

$$\omega_0 = \frac{1}{\sqrt[4]{L_R C_R L_L C_L}} \tag{A.8}$$

The third degree of freedom provides control over the characteristic impedance, Z_c, of the cell at ω_0. For the balanced case, Z_c can be obtained as:

$$Z_c = \sqrt{\frac{L_R}{C_R}} = \sqrt{\frac{L_L}{C_L}} \tag{A.9}$$

The behaviour of the characteristic impedance over the whole frequency range is shown in Fig. A.7 for a unit cell with π-topology or in Fig. A.8 for a unit cell with T-topology. The real part of this impedance grows or decreases, respectively, away from ω_0 towards to the cut-off frequencies. So, other considerations should be

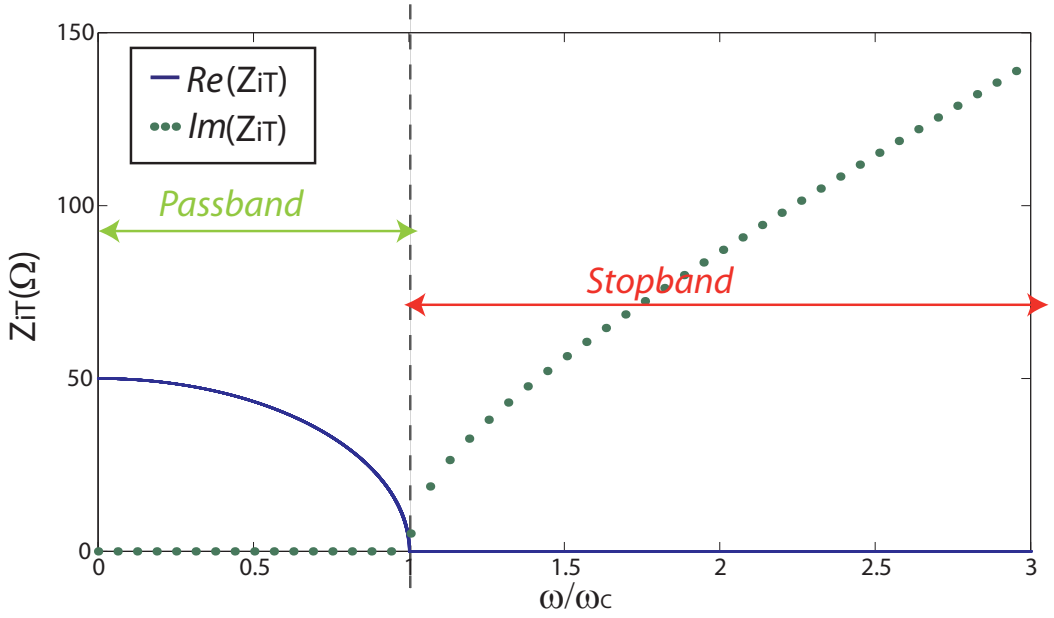


Figure A.4: Image impedance of a conventional RH-TL unit cell with T-topology

taken into account if a particular impedance value should be fixed aside from the ω_0 frequency. In that case, the equation listed in Table A.1 for the image impedance should be used.

Finally, the cut-off frequencies or the slope for the phase constant can be controlled by the last degree of freedom. Fig. A.10 shows the connection between them. The propagation constant for a balanced CLRH TL unit cell with three different slopes and the same ω_0 has been plotted. Please note how it is related to the values of their corresponding cut-off frequencies. The cut-off frequencies for the balanced case are given by the following equations:

$$\omega_{c1} = \omega_R \left| 1 - \sqrt{1 + \frac{\omega_L}{\omega_R}} \right| \tag{A.10}$$

$$\omega_{c2} = \omega_R \left(1 + \sqrt{1 + \frac{\omega_L}{\omega_R}} \right) \tag{A.11}$$

being $\omega_R = \frac{1}{\sqrt{L_R C_R}}$ and $\omega_L = \frac{1}{\sqrt{L_L C_L}}$.

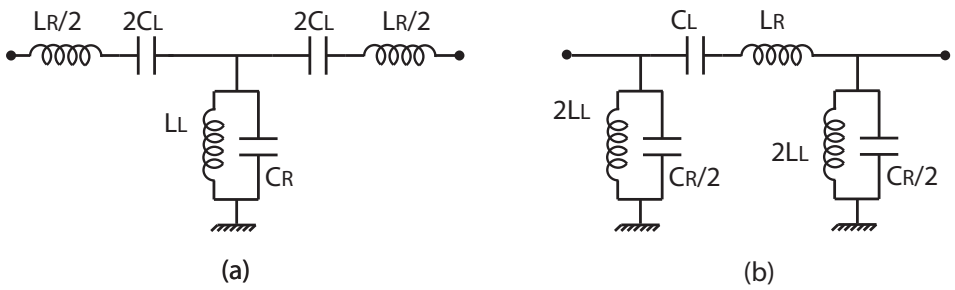


Figure A.5: CRLH unit cell with (a) T- and (b) π-topology

A.3 Periodically loaded transmission line

To analyze a periodically loaded transmission line we will consider an ideal transmission line with characteristic impedance $Z_0 = \sqrt{L/C}$, propagation constant $\gamma = j\beta = j\omega\sqrt{LC}$, and a ABCD matrix given by

$$\begin{bmatrix} v_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} \cos\frac{\theta}{2} & jZ_0 \sin\frac{\theta}{2} \\ j\frac{1}{Z_0}\sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix} \begin{bmatrix} v_{out} \\ I_{out} \end{bmatrix} \tag{A.12}$$

to which an element in parallel, Y, has been periodically added (see Fig. A.11). Since the line has now a given periodicity, it is possible to define an elemental cell in its T or π form (see Fig. A.12. If, for instance, the T-cell is considered, the network can be obtained by cascading the corresponding $ABCD$ matrices of the transmission line sections and the element in parallel, which is defined by [34]

$$\begin{bmatrix} \cos\frac{\theta}{2} & jZ_0 \sin\frac{\theta}{2} \\ j\frac{1}{Z_0}\sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \begin{bmatrix} \cos\frac{\theta}{2} & jZ_0 \sin\frac{\theta}{2} \\ j\frac{1}{Z_0}\sin\frac{\theta}{2} & \cos\frac{\theta}{2} \end{bmatrix} \tag{A.13}$$

and can be multiplied to obtain

$$\begin{bmatrix} \cos\theta + j\frac{\overline{Y}}{2}\sin\theta & Z_0(j\sin\theta - \overline{Y}\sin^2\theta) \\ \frac{1}{Z_0}(j\sin\theta + \overline{Y}\cos^2\theta) & \cos\theta + j\frac{\overline{Y}}{2}\sin\theta \end{bmatrix} \tag{A.14}$$

where $\overline{Y}$ is normalized to Y_0. From equation (A.14) it can be inferred that the unit cell with T-Topology has a new propagation constant θ' and characteristic

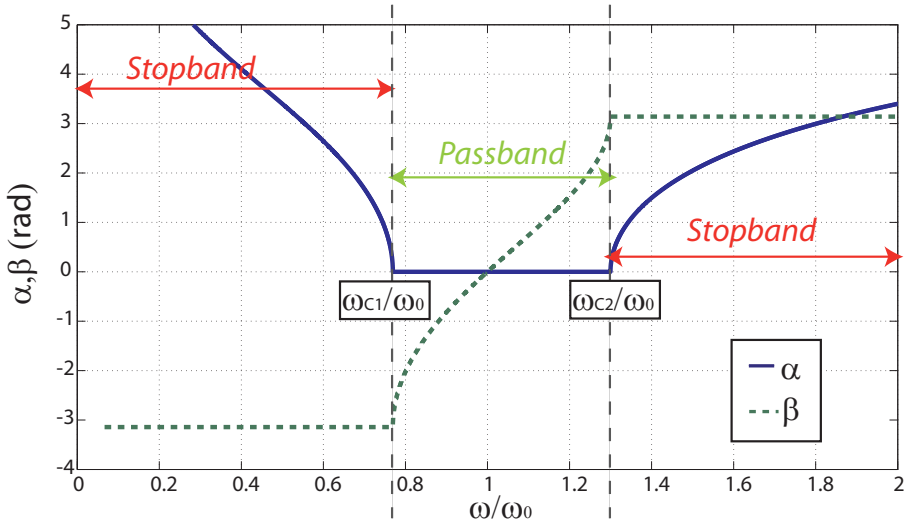


Figure A.6: Propagation constant of a CRLH-TL unit cell

impedance Z_0' given by

$$\cosh\theta' = \cos\theta + j\frac{\overline{Y}}{2}\sin\theta \tag{A.15}$$

$$Z_0' = Z_0\sqrt{\frac{\sin\theta + j\overline{Y}\sin^2\theta}{\sin\theta - j\overline{Y}\cos^2\theta}} \tag{A.16}$$

By analyzing the preceding equations, it can be seen that the transmission network now presents stopbands. In addition, the characteristic impedance is now frequency dependent. In a distributed amplifier Y is the admittance that corresponds to a capacitance, in this case, the behaviour of the unit cell will be quite similar to a RH-TL as described in the previous section (see Fig. A.3). From a design point of view, to correctly absorb a capacitance in a transmission line, equations (A.15) and (A.16) can be used to modify the characteristic impedance, Z_0 and the phase shift, θ, of the transmission lines sections between active devices to maintain the wanted values, now θ' and Z_0', within the desired bandwidth (the appearance of stopbands has now to be considered as well).

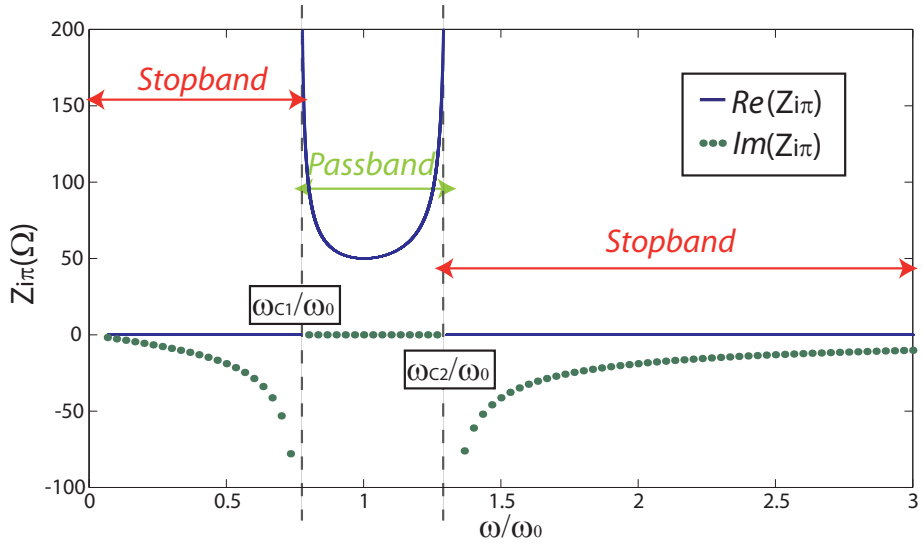


Figure A.7: Image impedance of a CRLH-TL unit cell with π-topology

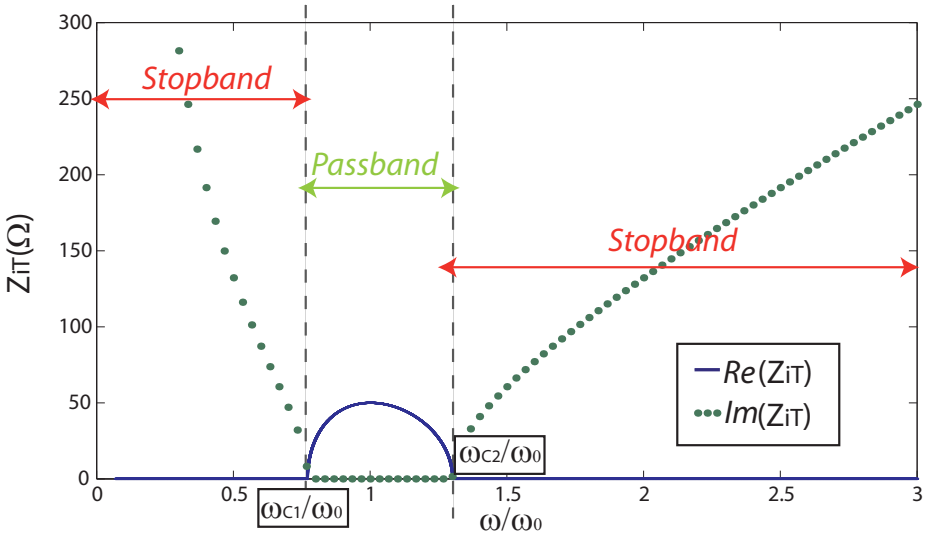


Figure A.8: Image impedance of a CRLH-TL unit cell with T-topology

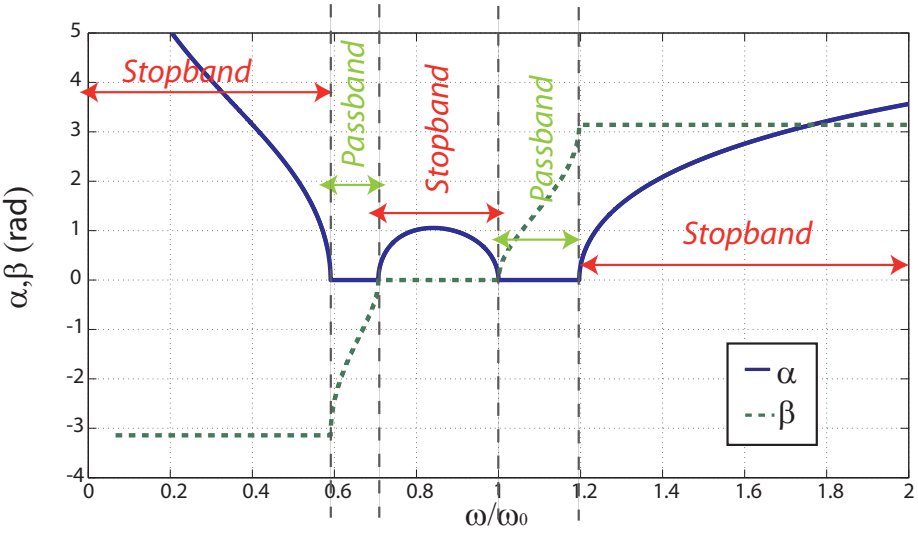


Figure A.9: Propagation constant of an unbalanced CRLH-TL unit cell

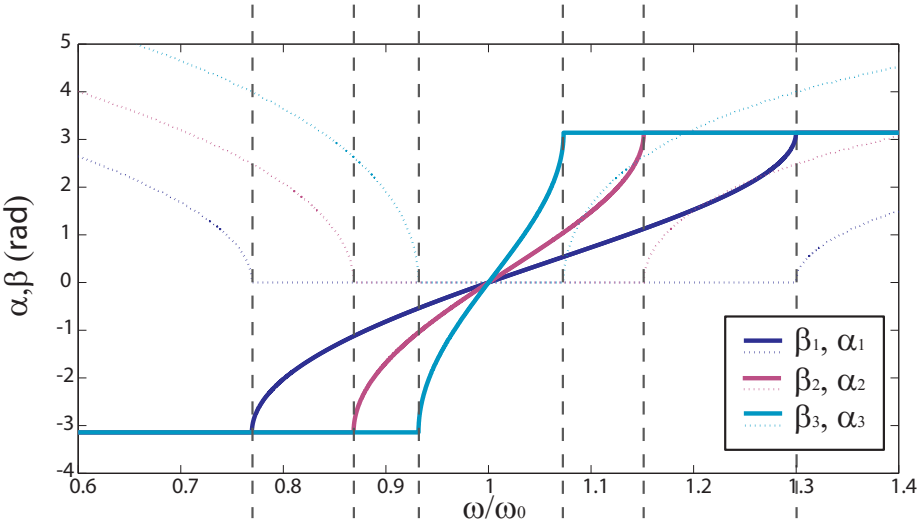


Figure A.10: Propagation constants (β: full line, α: dotted line) for a balanced CRLH-TL unit cell with three different slopes

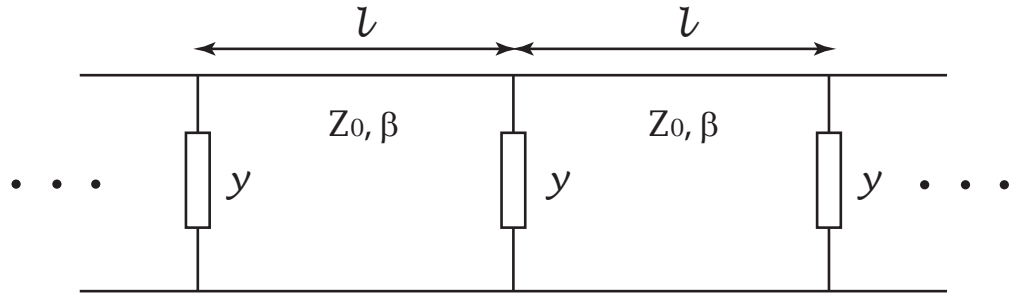


Figure A.11: Periodically loaded transmission line

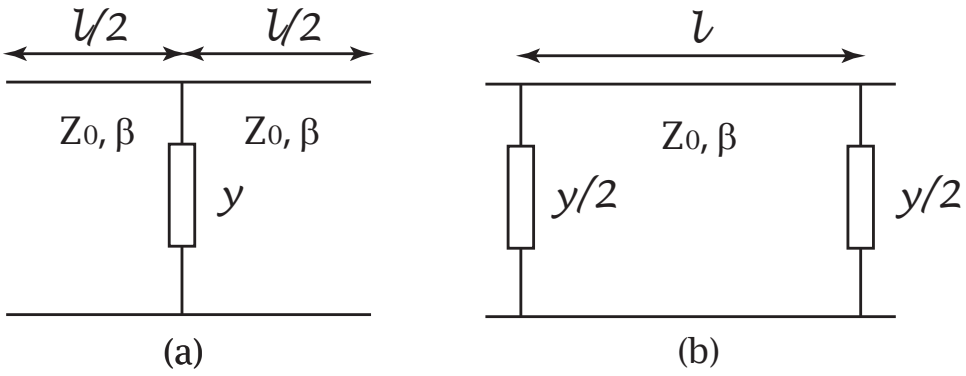


Figure A.12: Periodically loaded transmission line unit cell with (a) T- or (b) π-Topology

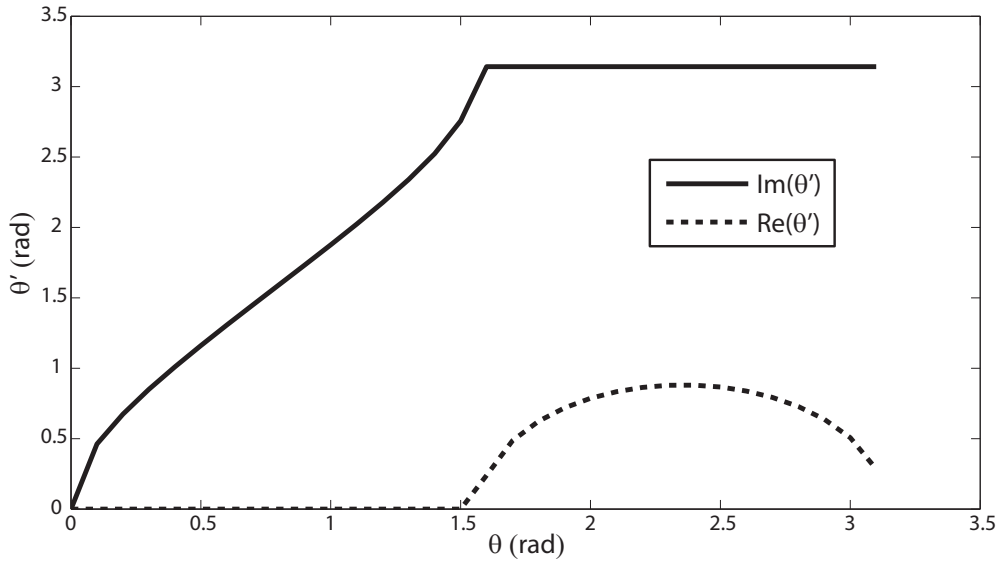


Figure A.13: Dispersion diagram for a lossless transmission line periodically loaded with a capacitance ($\overline{y} = j$, imaginary part in full line and real part in dashed line).

Appendix B

Power coefficients for a directional coupler in a power recycling configuration

In this Appendix the calculation of the power coefficients shown in Fig. 3.1 for a generic power recycling distributed amplifier is shown analytically, where losses and mismatch in the gate line have been considered. Firstly, the S parameters for a generic distributed amplifier are presented. For the analysis, an unilateral model for the active device and a continuous model for the transmission lines (including losses) have been taken into account. The reference impedance for the distributed amplifier is Z_g for ports 1 and 2 (gate line), and Z_d for ports 3 and 4 (drain line), whilst is Z_0 for the directional coupler and the auxiliary lines. Both Z_g and Z_0 are considered to be real impedances. Equations defining the 4-port distributed amplifier are given by:

$$S_{11} = S_{22} = 0; S_{12} = S_{21} = e^{-\gamma_{g\_line}L} \tag{B.1}$$

$$S_{33} = S_{44} = 0; S_{34} = S_{43} = e^{-\gamma_{d\_line}L} \tag{B.2}$$

$$S_{13} = S_{14} = 0; S_{24} = S_{23} = 0 \tag{B.3}$$

$$S_{31} = S_{42} = \frac{g_m \sqrt{Z_d Z_g}[e^{-(\gamma_{g\_line}+\gamma_{d\_line})} - 1]}{2(\gamma_{g\_line} + \gamma_{d\_line})} \tag{B.4}$$

$$S_{32} = S_{41} = \frac{g_m \sqrt{Z_d Z_g} e^{-\gamma_{d\_line}}[e^{-(\gamma_{g\_line}-\gamma_{d\_line})} - 1]}{2(\gamma_{g\_line} - \gamma_{d\_line})} \tag{B.5}$$

where g_m is the transconductance of the transistor and γ_{g_line} and γ_{d_line} are the propagation constants of the gate and drain lines, respectively.

The reference impedance in the gate line can be renormalized to Z_0 by applying this conversion equation [50]:

$$[S'] = [A]^{-1} \cdot ([S] - [R]) \cdot ([I] - [R] \cdot [S])^{-1} \cdot [A] \tag{B.6}$$

where

- $[S]$ the original S-parameter matrix
- $[S']$ the renormalized scattering matrix
- $[I]$ the identity matrix
- $[R] = \begin{pmatrix} r(Z_1) & 0 & \cdots & 0 \\ 0 & r(Z_2) & \cdots & 0 \\ \vdots & \vdots & \ddots & \cdots \\ 0 & 0 & \cdots & r(Z_N))) \end{pmatrix}$
  with $r(Z_n) = \dfrac{Z_n - Z_{n,before}}{Z_n + Z_{n,before}}$, and $Z_{n,before}$ and Z_n the reference impedances of port n before and after the normalizing process, respectively.
- $[A] = \begin{pmatrix} A_1 & 0 & \cdots & 0 \\ 0 & A_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \cdots \\ 0 & 0 & \cdots & A_N)) \end{pmatrix}$

$$\text{with } A_n = \sqrt{\frac{Z_n}{Z_{n,before}}} \cdot \frac{1}{Z_n + Z_{n,before}}$$

which leads to the following S-parameters for the gate line after the normalization:

$$S_{11} = S_{22} = \frac{(1 - X^2)\Gamma}{1 - \Gamma^2 X^2} \tag{B.7}$$

$$S_{12} = S_{21} = \frac{(1 - \Gamma^2)X}{1 - \Gamma^2 X^2} \tag{B.8}$$

where $\Gamma = \frac{Z_g - Z_0}{Z_g + Z_0}$ and $X = e^{-(\alpha_{g\_line}L + j\theta_{g\_line})}$.

This new scattering matrix can now be used to calculate the power coefficients described in Fig. 3.1 through the following equations:

$$b_5 = \frac{-jA \cdot a_6}{1 + jB \cdot S_{21} \cdot e^{-j(\theta_{aux1} + \theta_{aux2})} + \frac{S_{22} \cdot S_{11} \cdot B^2 \cdot e^{-2j(\theta_{aux1} + \theta_{aux2})}}{(1 + jB \cdot S_{12} \cdot e^{-j(\theta_{aux1} + \theta_{aux2})})}} \tag{B.9}$$

$$a_5 = \frac{S_{11} \cdot b_5 \cdot e^{-j(\theta_{aux1} + \theta_{aux2})}}{(1 + jB \cdot S_{12} \cdot e^{-j(\theta_{aux1} + \theta_{aux2})})} \tag{B.10}$$

$$b_6 = -jA \cdot a_5 \tag{B.11}$$

$$b_7 = -jB \cdot a_5 \tag{B.12}$$

$$a_7 = S_{21} \cdot b_5 \cdot e^{-j(\theta_{aux1} + \theta_{aux2})} + S_{22} \cdot b_7 \cdot e^{-j(\theta_{aux1} + \theta_{aux2})} \tag{B.13}$$

$$b_8 = jB \cdot a_6 - jA \cdot e^{-j(\theta_{aux1} + \theta_{aux2})}(S_{21} \cdot b_5 + S_{22} \cdot b_7) \tag{B.14}$$

Appendix C

High-efficiency power amplifier design: experimental results

To validate the theory set out in chapter 5, the design and manufacture of several power amplifiers have been assessed. A GaN HEMT active device has been selected for the design.

C.1 GaN transistor-based harmonic-tuned power amplifier for the low L-band

In this subsection the description of the designing, building and measuring process of a harmonic-tuned power amplifier for the low L-band applications has been carried out [51]. It includes the technological aspects of the design and measurements under three different type of excitation: CW, a two-tone signal and a scaled version of the E5 Galileo's AltBOC modulation scheme [52; 53].

C.1.1 Circuit Design

The amplifier design, which was aimed to be working in Class E mode, has been made by using the widely-known closed-form design equations for a Class E working condition [54]. The CGH35015F GaN high electron mobility transistor has been selected. The physical device characteristics, required for the design process, were extracted from the AWR's model provided by the device's manufacturer, CREE®. Microstrip technology has been selected for the manufacture of the prototype, using a 1mm FR-4 substrate.

Both the fundamental and the harmonics were modified, compared to the values obtained from the analysis in Class E, after doing a load-pull analysis based on the manufacturer's model. Appropriate output waveform shaping has been made possible thanks to the use of a multi-harmonic matching network, including stubs for the second and the third harmonic, whilst using a lumped capacitor for the adjustment of the fundamental. For the input matching network, only the fundamental excitation tone has been considered, by using, as in the output case, a lumped capacitor since it allows *in situ* circuit adjustment. The design has been made for the L-band applications, with a centre frequency @ $f_0 = 1191.795MHz$ (the so-called Galileo E5 band centre frequency). Fig. C.1 shows a photograph of the developed Class E GaN HEMT amplifier. Fig. C.2 shows the microwave facilities at the University of Malaga.

C.1.2 Measurements

The designed amplifier, as expected, behaves properly when working with constant envelope modulation formats. The measurements presented below include CW measurements at the E5 band centre frequency, f_0, a two-tone test and measurements taken with a scaled version of the modulated E5 signal adjusted to the bandwidth limitations of the available IQ demodulator. The instrumentation set-up includes an Agilent E4448A Spectrum Analyzer, the Agilent Signal Generator E8267D, and the Agilent Signal Generator N9310A. The AltBOC base-band signal has been generated using the Matlab® environment using an appropriate adaptation of the algorithm developed and proposed in [53].

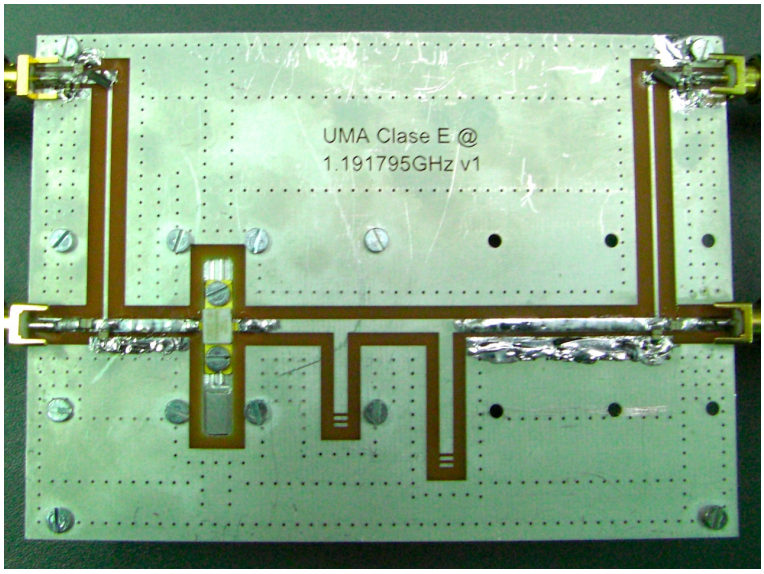


Figure C.1: Class E GaN HEMT amplifier prototype

CW Measurments: The continuous wave measurements have been taken for the centre operation frequency. At this frequency and with the following bias conditions, $V_{GS} = -2.8V$ and $V_{DS} = 36V$, the amplifier provides 15W output power, a 75% output efficiency and a 74% PAE (Fig. C.3). The measured results are consistent with simulations.

Two-tone test: The intermodulation distortion (IMD) behavior has also been characterized using a two-tone test (centered f_0, $\Delta f = 10kHz$). The results are presented in Fig. C.4. The measured profile, showing a large signal sweet-spot, corresponds to the selection of a class C operation point.

Modulated signals: A constant envelope (AltBOC) modulation in the low L-band (Galileo's E5 band) was finally selected in order to evaluate the amplifier's performance under modulated signals. The bandwidth of the original Galileo signal, which is centered at 1191.795 MHz and occupies around 51 MHz (the first two lobes), has been scaled-down to 450 kHz in order to adapt it to the available transmission and reception capabilities of our characterization set-up. Considered as the most sophisticated signal from among all that have been designed for the Galileo Navigation Satellite System, the E5 signal is a compound of four codes modulated

Figure C.2: Measurement set-up

into the two phases of the orthogonal sub-carriers. The selection of the constant envelope AltBOC modulation establishes the sub-carrier waveforms, which must be chosen in order to maintain the signal's constant envelope. The theoretical power spectrum of the E5 signal is therefore a split spectrum around the center frequency, f_0 [53]. The spectrum of the amplified E5 signal has been captured for three different input power levels. The traces have been plotted in Fig. C.5. Here it is noticeable that the power spectrum density of the modulated signal maintains a good resemblance even for the highest input power levels of the signal. To cover a complete characterization of the amplifier, the efficiency of the implemented device

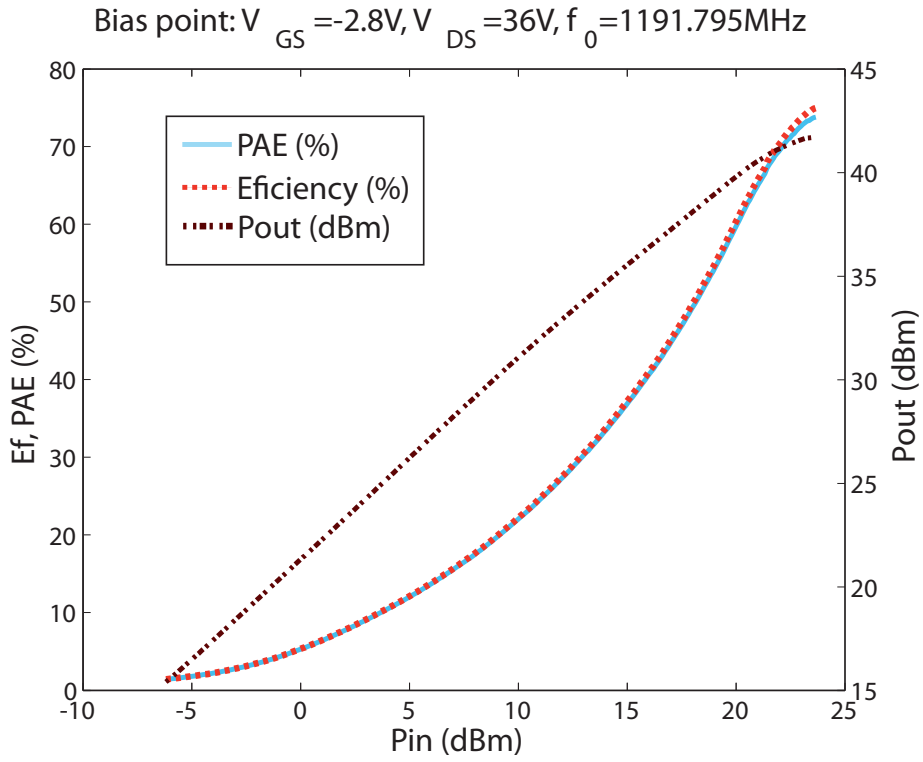


Figure C.3: Measured output power, efficiency and PAE.

has been measured under the modulated signal excitation proposed above. The trace, presented in Fig. C.6, has been plotted against the average input power of the scaled-down Galileo's signal. The results are quite close to that obtained for the CW signal reaching a 70% PAE. A representation of the constellation for the received scaled E5 signal is plotted both in Figs. C.7 and C.8. Amplitudes of the received and transmitted symbols have been normalized to their maximum for fair comparison. Pictures have been taken for different input power levels showing similar results, in all the cases, to the original signal, showing again the good behavior of the amplification stage under this kind of excitation. In Fig. C.9 there is a picture of the amplified signal's envelope where its constant nature can be appreciated. The peak-to-mean relationship after an average process has given a result of less than 1 dB. Finally, the performance of the amplifier has been assessed through a comparison of how it behaves under other modes of operation. For this reason the $V_{GS} = -2.3V$ and $V_{DS} = 36V$ bias point has been chosen, which stands between

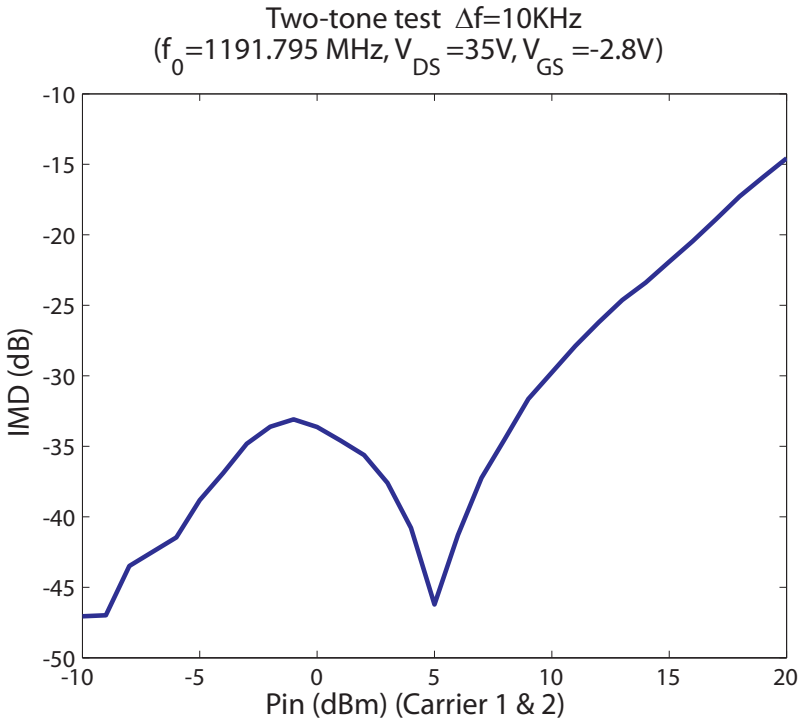


Figure C.4: Measured intermodulation distortion.

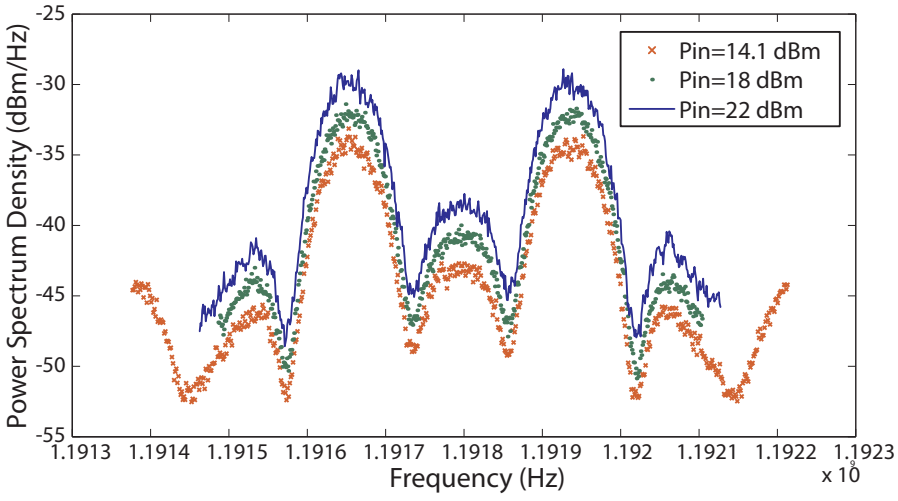


Figure C.5: Measured Power Spectrum Density for different input power (rms) levels.

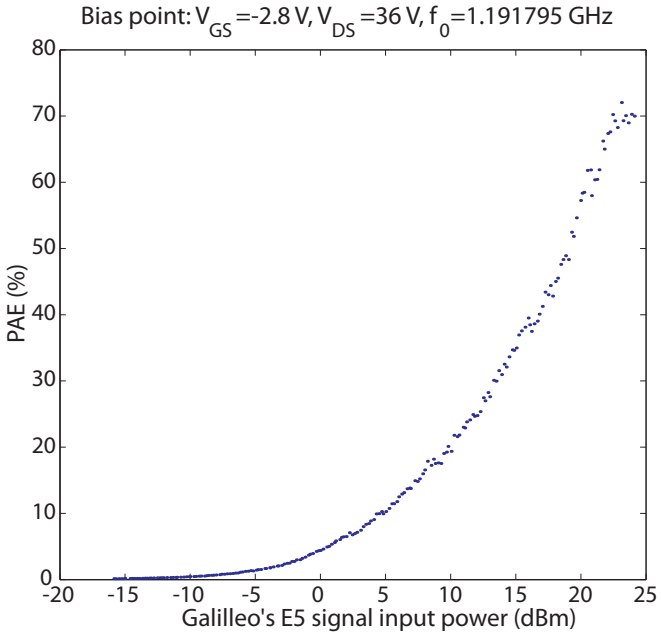


Figure C.6: Measured PAE under the Galileo's E5 modulated signal.

the B and AB biasing regions. Figures C.10 and C.11 correspond to CW excitation whereas figure C.12 shows the amplifier response under modulated signal excitation. The results are similar to the Class E mode, achieving a little less efficiency both in the CW and modulated signal cases, around a 70% PAE. The constellation capture for this operation point has also given a reasonable result even for the highest input power levels.

C.2 Class E power amplifier at 3.5 GHz

The design, manufacturing and measurement of a Class E power amplifier with multi-harmonic shaping for the operation frequency of 3.5 GHz is described in this subsection. The work has been done in conjunction with the Communication Engineering Department[1] of the University of Cantabria.

The selected active device was the CREE GaN HEMT CGH35015 (Fig. C.13). The design flow is based in the well-known theory for Class E power amplifier design.

[1]Microwaves and Radiocommunication Systems Group

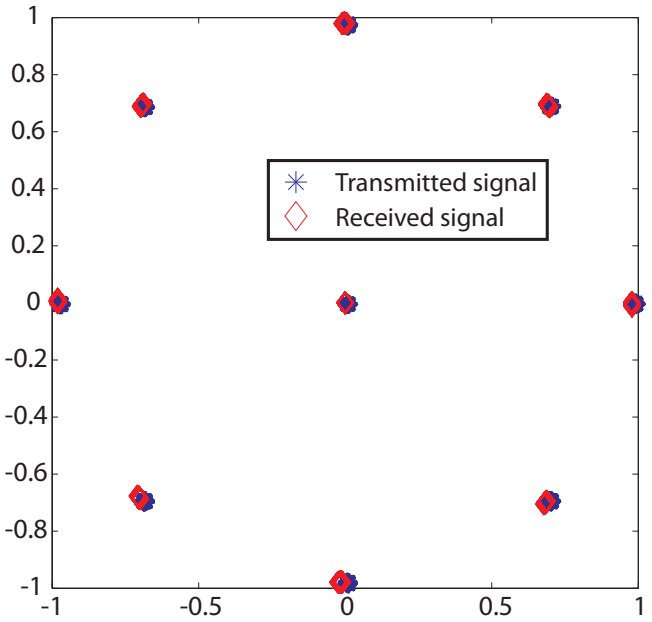


Figure C.7: Normalized Galileo's E5 signal constellation (Pin=4 dBm).

The process requires the selection of the bias point and the matching of the output and the input, which has been done in two different phases.

The bias point must be chosen close to the cut-off region, which has been found through the analysis of the large signal model of the active device provided by the manufacturer. The final selected bias point has been $V_{GS} = -2.7V$ and $V_{DS} = 28V$.

Firstly, the output matching has been assessed. The fundamental load is selected according to the equations obtained by imposing the conditions for a Class E mode of operation (5.26). This value has been modified through a load pull simulation to find the better performance in terms of output power and efficiency. In Fig. C.14 it can be observed that the maximum output power and efficiency are not coincident, and in this design preference has been given to the efficiency performance. The harmonic components have also been studied, instead of imposing the open circuit dictated by Class E theory. A load pull analysis has been made for the second (Fig. C.15) and the third harmonics and it can be seen that both of them are close to the open circuit.

Secondly, a load pull analysis is carried out in the input of the active device to

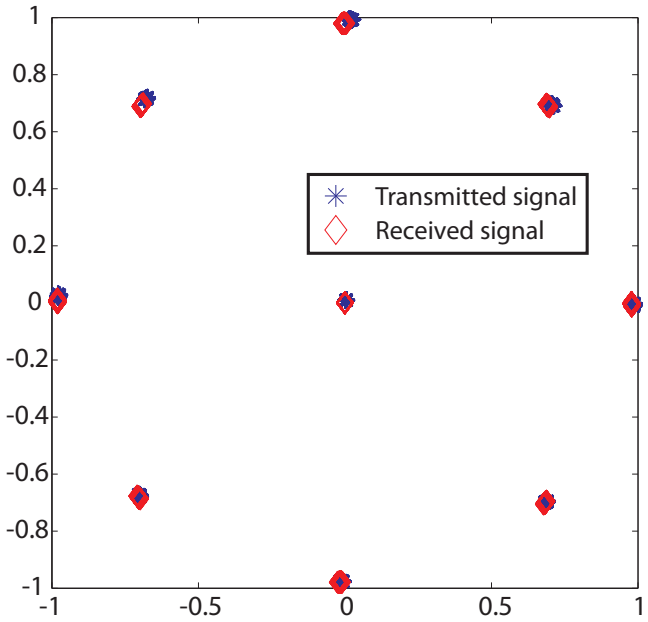


Figure C.8: Normalized Galileo's E5 signal constellation (Pin=24 dBm).

achieve the better performance in terms of gain. In Fig. C.16 the different contours for output power and efficiency are plotted for the different input impedances for the fundamental frequency and it can be observed that the maximum for both magnitudes are coincident.

Once the load conditions for the input and output of the active device have been selected, the gain and the PAE versus the input power has been plotted for different V_{DS} values (see Fig. C.17). It can been seen that, indeed, by applying the previous load conditions and the selected gate to source voltage the amplifier works as a switch. The gain increases for high input power levels. The PAE has a maximum of 74% and the gain can achieve 12 dB.

The design of the multi-harmonic matching network has been made with several stubs and the number of vias has been increased in the proximities of the lumped elements to prevent electromagnetic fields coupling. The layout has been prepared to fit an aluminum base that serves as a heat sink (Fig. C.18).

The manufactured prototype is presented in Fig. C.19 and an image of the work area in the Communication Engineering Department of the University of Cantabria

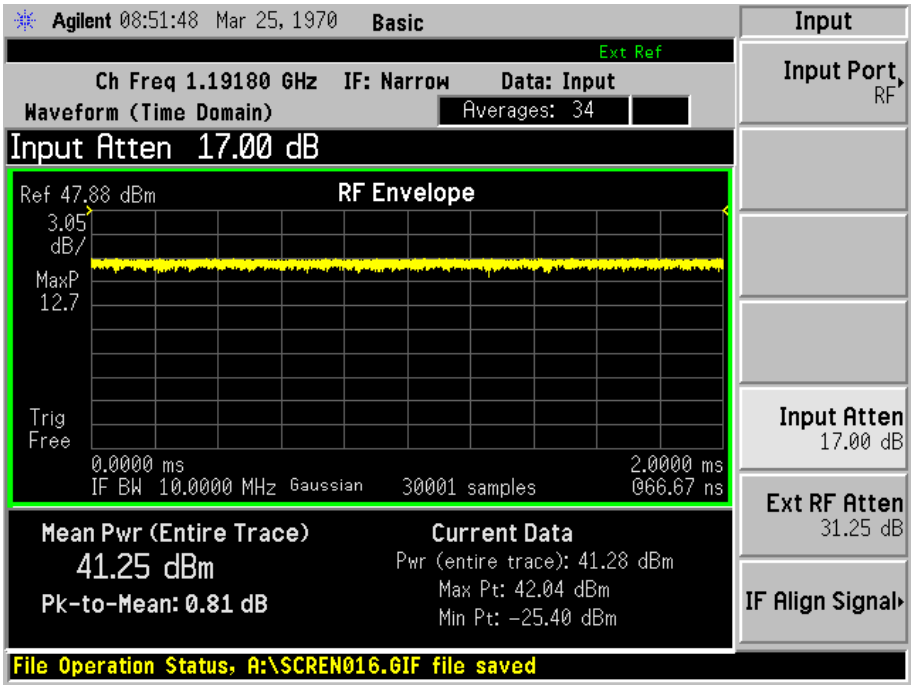


Figure C.9: Amplified E5 signal's envelope (Pin=24 dBm).

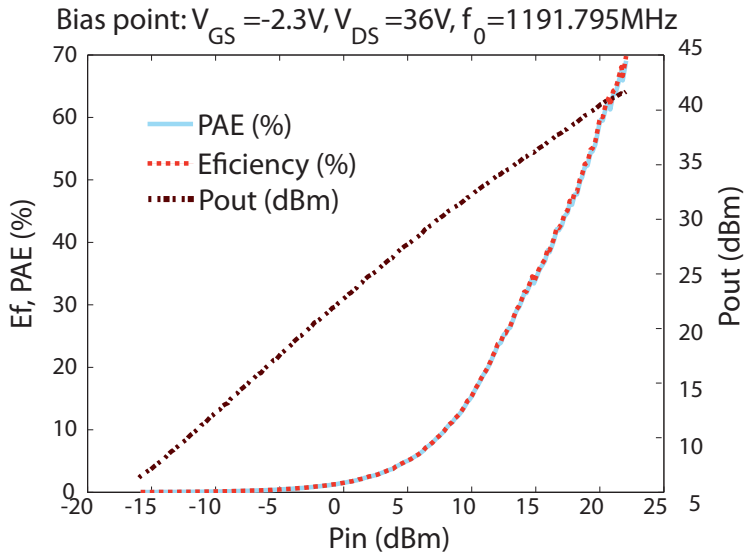


Figure C.10: Measured output power, efficiency and PAE. Class AB biasing point.

is shown in Fig. C.20. Measurement results provided a 54% drain efficiency, a 13W output power performance , a 12dB gain and a 51% PAE for a $V_{DS} = 28V$ and

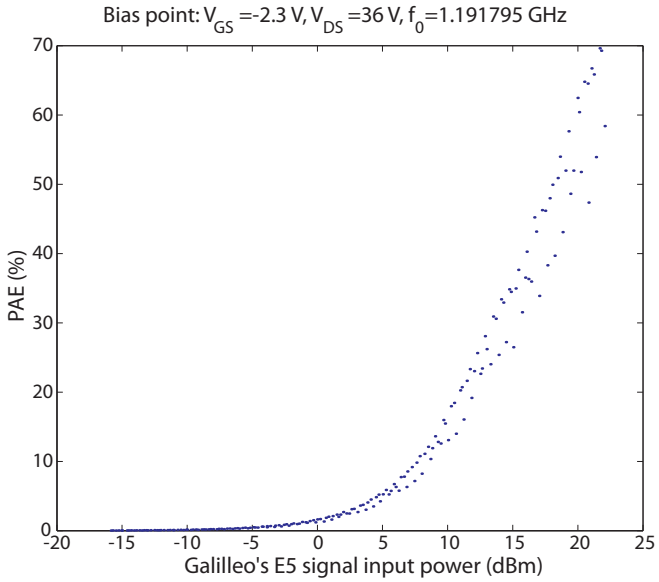


Figure C.11: Measured PAE under Galileo's E5 modulated signal. Class AB biasing point.

$V_{GS} = -3V$ bias point. By increasing the drain to source voltage up to 35V the available output power of 15W were retrieved from the active device at the expense of a drop in the efficiency performance.

The amplifier was excited with a WiMAX signal with a 500kHz bandwidth. After a frequency sweep it could be found that the optimum frequency point was 3.42GHz, so the measurements were taken for this value. In Figs. C.21 and C.22 the output power spectrum for a WiMAX signal has been plotted for different input power values, where it can be seen that the designed amplifier is able to amplify complex signal modulations schemes successfully. The measured EVM is a little high, 13.9%, which could be solved by adding predistortion techniques.

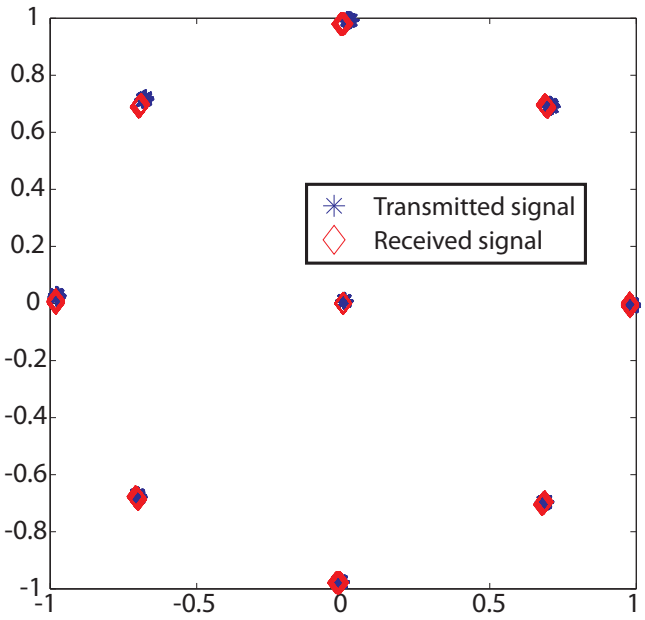


Figure C.12: Normalized Galileo's E5 signal constellation (Pin=24 dBm, Class AB biasing point).

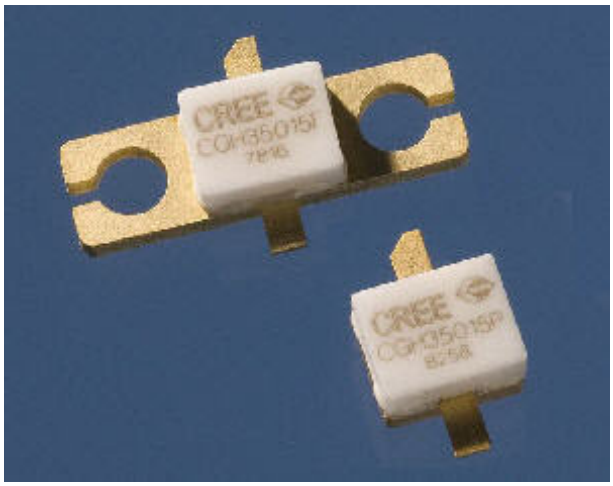


Figure C.13: CGH35015 GaN transistor

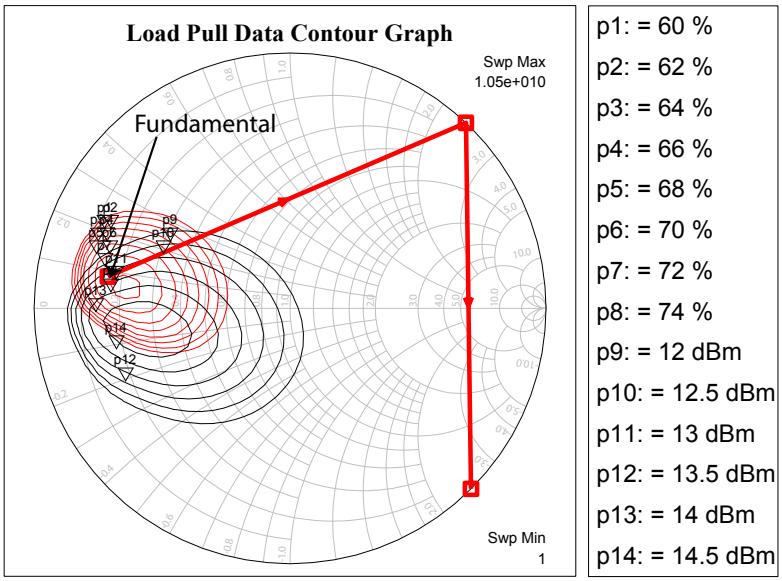


Figure C.14: Simulated load pull output power (black) and efficiency (red) contours for a GaN HEMT (Cree, CGH35015F) at the fundamental load of 3.5 GHz.

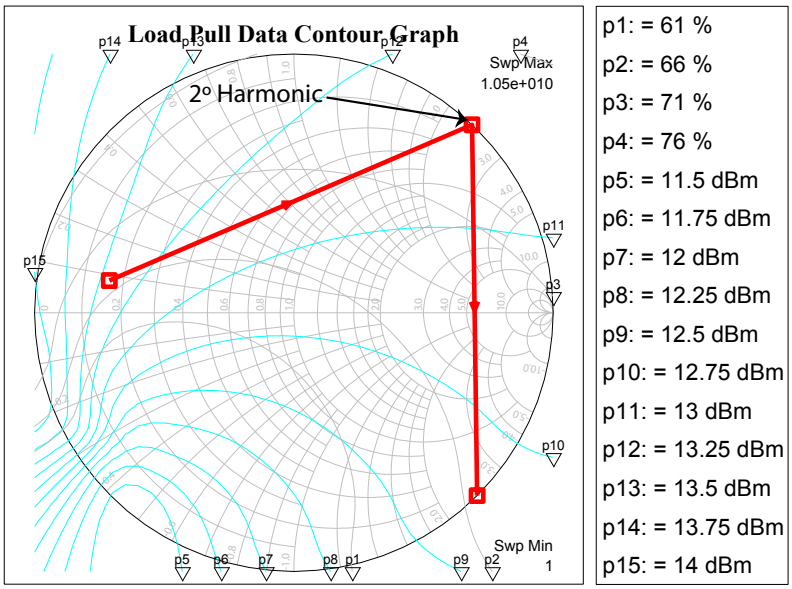


Figure C.15: Simulated load pull output power (blue) and efficiency (gray) contours for a GaN HEMT (Cree, CGH35015F) at the second harmonic.

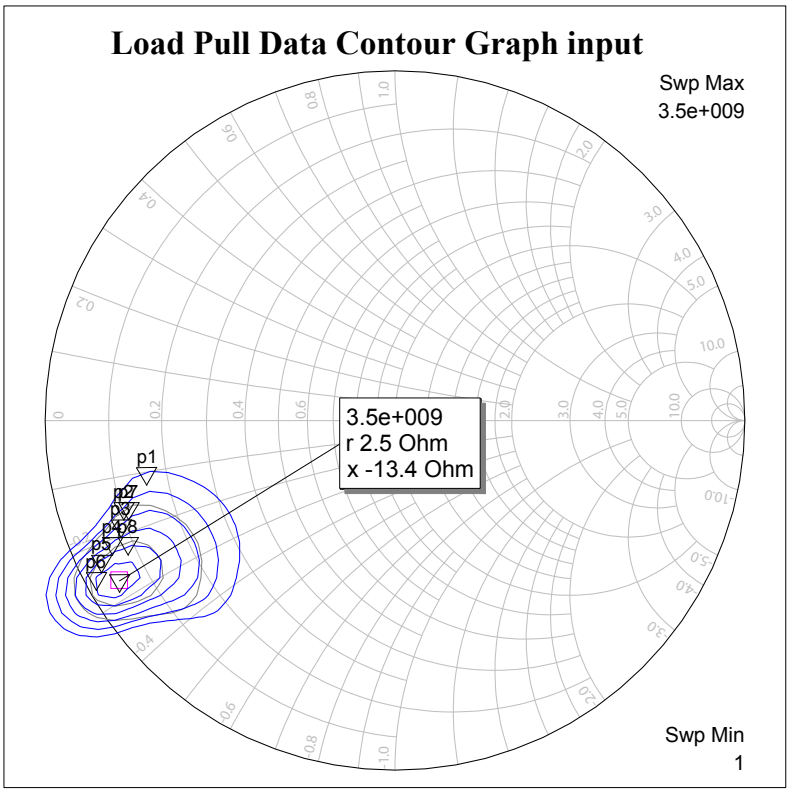


Figure C.16: Simulated load pull gain (gray) and efficiency (blue) contours for a GaN HEMT (Cree, CGH35015F) at the fundamental input load.

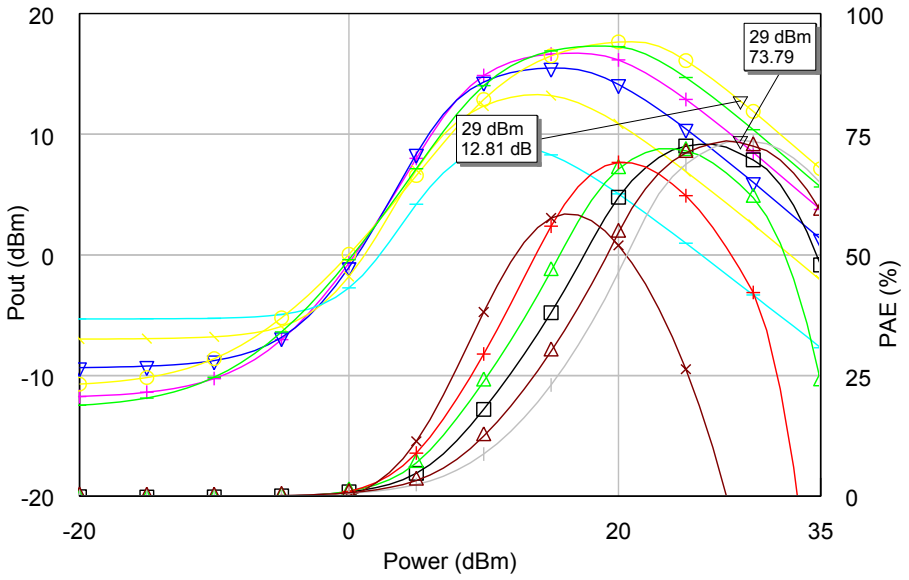


Figure C.17: Simulated gain and PAE versus input power for different V_{DS} values at the fundamental frequency of 3.5 GHz

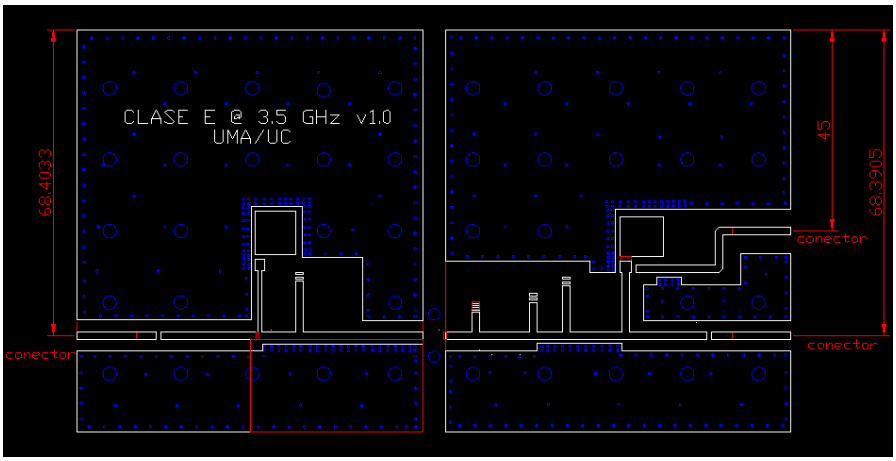


Figure C.18: Final layout of the designed Class E power amplifier for 3.5 GHz

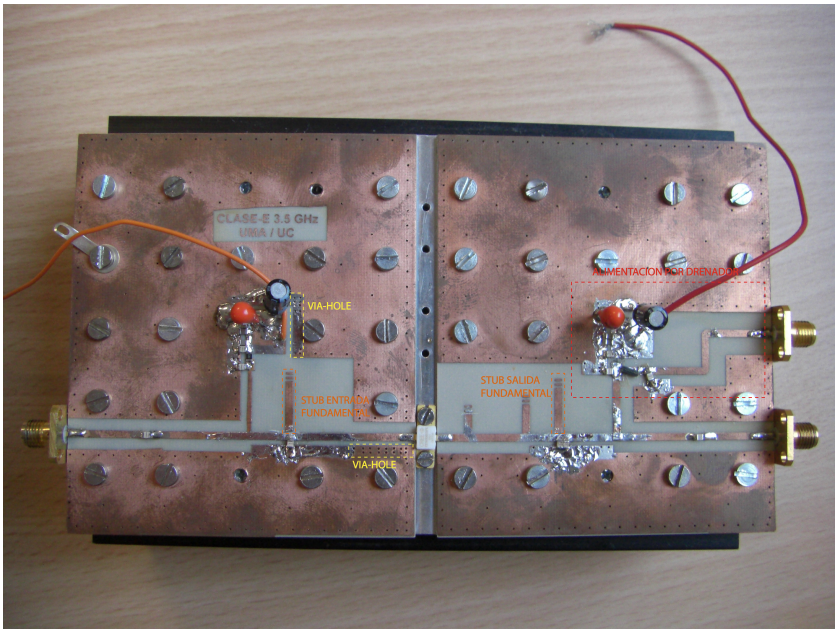


Figure C.19: Class E power amplifier for 3.5 GHz

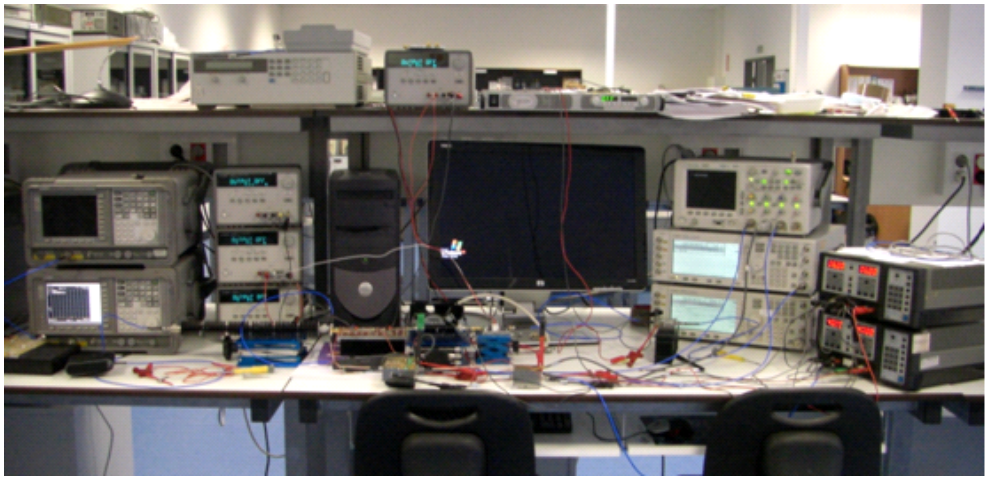


Figure C.20: Workbench at the Microwaves and Radiocommunication Systems Eng. group of the Communications Engineering department of the University of Cantabria

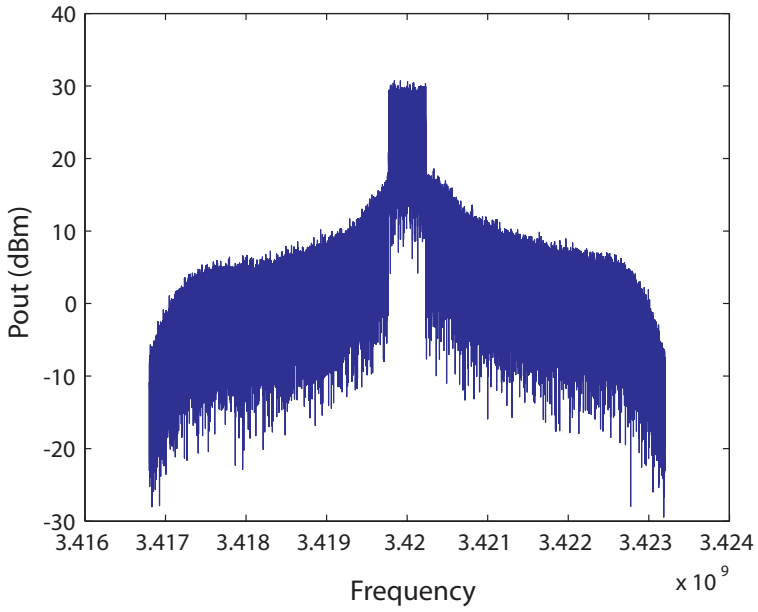


Figure C.21: Output power spectrum for a WiMAX signal (500kHz bandwidth) versus frequency for a 29.69 dBm input power

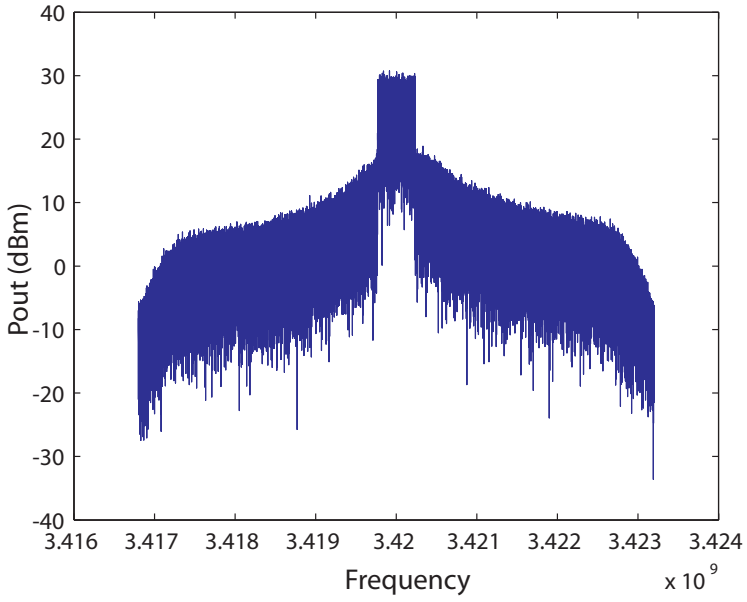


Figure C.22: Output power spectrum for a WiMAX signal (500kHz bandwidth) versus frequency for a 31.47 dBm input power

Appendix D

Manufacturing and measurement resources

This appendix provides an overview of the software tools, measurement capabilities and manufacturing technology that have been used for the preparation of this PhD thesis.

D.1 RF/microwave design software

RF microwave design CAD tools are computer-aided design (CAD) software platforms specifically developed to aid in the design, modeling, and simulation of an RF or microwave product. It is a visual and symbol-based method of communication whose conventions are particular to RF/microwave engineering.

Among the many design CAD tools that can be found it is worth noting some of the most popular ones such as Microwave Office, Advanced Design System or Ansoft's HFSS. For the work developed in this Thesis, Microwave Office has been selected. Built on the AWR high-frequency design environment platform, it encompasses all the tools essential for high frequency IC, PCB and module design, including linear and non-linear circuit simulators, electromagnetic (EM) analysis tools and integrated schematic and layout.

D.1.1 Linear circuit simulator

The linear simulator is used to analyze a schematic if all the elements within it are linear. It is based on the nodal admittance matrix method.

D.1.2 Non-linear circuit simulator

For non-linear simulation the Harmonic Balance (HB) method is used. The method constitutes a powerful technique for the analysis of high-frequency non-linear circuits such as mixers, power amplifier, and oscillators. The fast development of the method since the early 1990s currently allows the application of the method to very large non-linear circuits, and circuits that process complicated signals made up of hundreds of spectral components.

D.1.3 EM simulation

Performing EM simulations constitutes an important final step during the design process since it allows possible coupling effects between the elements of the circuit and the degree of accuracy of the circuital models used in previous design steps to be checked.

For this task, the AWR's AXIEM EM software has been selected. The product has been developed specifically for three-dimensional (3D) planar applications such as RF PCBs and modules, LTCC, MMIC and RFIC designs.

AXIEM^{TM} is a Method of Moments solver that solves for the currents on conductors that can be embedded in a stackup of planar dielectric layers. An interesting feature of the software resides in the integration between the circuital and the electromagnetic simulation. By using the "Extraction block" it is possible to carry out an EM simulation based on the layout associated to the electrical model of the component. The results of this simulation are automatically merged back into the schematic and the simulation of the entire schematic is then carried out. A previous definition of the stackup is mandatory. This option allows full integration of non-linear and EM simulations, by taking into account coupling effects in schematics that may contain active elements.

D.1.4 PCBs design

A preliminary layout can be directly extracted from Microwave Office thanks to its layout module, that uses an object-oriented design database to manage the association between schematics and layout. Each electrical component in a schematic is assigned a layout representation. The layout representation is used to create the physical Layout View of each electrical component in the schematic. Since the electrical component and the layout representation are treated as a single object, any changes to the electrical object are immediately reflected in the layout object and vice-versa. This close association between the electrical component and the layout representation virtually eliminates the time-consuming and error-prone back-annotation that is typically required to synchronize schematics and layouts in other systems. In a second iteration, the layout is imported to AutoCAD where the finishing touches are made before sending it to the foundry.

D.2 Measurement capabilities

Below is detailed and briefly described the instrumentation that has been used to take the measurements presented in this Thesis:

- The agilent E4448A PSA Series Spectrum Analyzer measures and monitors complex RF, microwave, and millimeter-wave signals up to 50GHz. It has a 10MHz analysis bandwidth. It can be controlled via LAN or GPIB.
- The agilent E8267D PSG Vector Signal Generator provides an RF signal up to 44 GHz and 23dBm output power. Among its modulation capabilities there are several options such as analog AM,FM or pulse modulations and digital modulations such as ASK, FSK, QAM or custom I/Q. Its internal baseband generator has a 80MHz RF bandwidth and allows arbitrary waveform and real-time I/Q. It can be controlled via LAN or GPIB.
- The agilent E8364A PNA Series Network Analyzer with a frequency range between 45MHz and 50 GHz allows TRL calibration for waveguide, on-wafer, and in-fixture devices. The power level from the test port can vary depending on the frequency range. It can be controlled via LAN or GPIB.

- The agilent N9310A RF Signal Generator has a frequency range between 9 KHz to 3 GHz, and an extensive analog modulation: AM, FM, Phase, and Pulse modulation. It can be controlled via GPIB.
- Agilent DC Power Supply: E3634A is a 200W Power Supply, with two different ranges, 25V - 7A or 50 - 4A; 6614C is a 50W System Power Supply with a 100V - 0.5A range; and 6612C is a 40W System with a 20V - 2A range.

D.3 Manufacturing technologies

D.3.1 Soldering basics

Soldering filler materials are available in many different alloys for differing applications. In electronics assembly, the eutectic alloy of 63% tin and 37% lead (or 60/40, which is almost identical in melting point) has been the alloy of choice. Soldering steps include:

- Contact of the solder to the parts to be joined.
- Slow application of heat to warm the parts to be soldered.
- Oxide removal from the joining surfaces and solder metallurgies.
- Application of the required heat to melt the solder.
- Solder wetting to joining surfaces and intermetallic formation.
- Quenching of the solder liquidus.

D.3.2 Electrically conductive epoxy

An electrically conductive epoxy is a conductive epoxy filled with electrical conductors such as nickel, tin, copper, gold and silver. Because epoxies themselves are bad conductors of heat and electricity as they are polymers, with the combinations of a hydrocarbon and polyamine, they cannot be used directly for industrial purposes

where thermal and electrical conductivity is required. However, this disadvantage of epoxies is countered by their ability to accept fillers.

An electrically conductive epoxy is available either as in two-parts or one. For a two part epoxy, the materials have to be mixed. Here is the catch. For the two-part epoxy, uniformity of the material is questionable because one has to be extremely careful about the quantities when mixing. The one part electrically conductive epoxy is available as premixed and degassed. They also come frozen in syringes. However, if the two-part epoxy is properly mixed, both demonstrate optimum flow properties.

An electrically conductive epoxy gives excellent adhesion for most of the metals. This also holds true for the plastic substrates. And this is because of their high temperature resistance and because they allow the two substrates that need to be bonded to have different thermal expansion levels. A property that is not very easily available in the method of joining parts by soldering. Just as of you are soldering bronze and copper together, the bond would not only require high levels of heat but would also, after some time, end up with the bond being slightly corroded in places. However, if you solder two copper pieces together, then not only is the bond easy to make but is also durable. The difference of quality is not an issue when dealing which electrical epoxies.

For the attachment of lumped elements in PCBs the choices in conductive epoxies are essentially two; silver and gold epoxy. Silver epoxy adhesives are one are the most widespread options and have been widely used in semiconductor and electronic packaging industries since the 1960s, as a reliable connection method instead of soldering or eutectic joining of metals.

A main advantage of the silver epoxy over the soldering techniques, which are nowadays based on *pure tin* or *tin-rich alloys*, is that it presents more ductility, the components are not exposed to such a high temperatures, and it is less inclined to "tin-whisker" formation, which is a conductive tin crystal which can spontaneously grow from tin based lead-free finished surfaces even at room temperature. However, what the epoxy adheres to needs to be chosen carefully. When used for electrical contacts, it is important that the metalization has similar potentials to avoid galvanic corrosion and non-conductive oxides.

Palladium, platinum and gold are noble metals which will not readily oxidize,

due to their electron orbital configuration. Silver is also a noble metal with a similar configuration, but will oxidize under the right conditions. However, even if the silver oxidizes, its oxides are conductive.

Lead and tin are main groups metals containing free electrons that will readily form non-conductive oxides and can cause serious conductivity issues. Since these oxides form on the surface of the metal, they can also significantly reduce the shear strength of an adhesive bond.

Silver epoxy should never be used on pre-tinned surfaces for three reasons.

- It is industry legacy and common sense that noble metals like to be joined to other noble metals.
- Silver and tin have dissimilar potentials, leading to galvanic corrosion, via a tarnish or rusting process.
- Silver itself can be a catalyst for tin whisker formation.

Pure tin should be avoided by plating components with materials that do not have a tendency to whisker, such as Au, Ag, AgPd, NiPdAu, Pt, Pd, Cu.

Appendix E

Resumen

E.1 Introducción

E.1.1 Marco contextual

La amplificación distribuida, que fue formulada por Percival en 1936 [1], se concivió como un medio para combinar la potencia de salida de varios dispositivos activos. En aquel momento, el desarrollo en el campo de la electrónica requería una optimización tanto de la ganancia como del ancho de banda. Percival descubrió que el producto ganancia-ancho de banda se encontraba fuertemente relacionado con la capacidad de salida del dispositivo activo y propuso una solución basada en la absorción de dichas capacidades por líneas de transmisión artificiales. El trabajo de Percival no tuvo impacto hasta una década más tarde cuando Ginzton *et al.* [2] extendieron este concepto. Señalaron las principales limitaciones de la amplificación distribuida en términos de ganancia y ancho de banda y propusieron varias estrategias para solventarlos. Ginzton *et al.* también consiguieron crear los primeros prototipos con buenos resultados [3]. Desde entonces, la amplificación distribuida se ha utilizado ampliamente para desarrollar amplificadores de banda ancha para un gran abanico de aplicaciones [4; 5; 6; 7].

En contraposición al rápido desarrollo de la amplificación distribuida en régimen

de gran señal, no fue hasta 1984 cuando el amplificador distribuido bajo condiciones de gran señal empezó a atraer cierta atención. En ese año Gamand *et al.* publicaron un artículo [8] donde llevaban a cabo un análisis de distorsión para explicar el comportamiento del amplificador distribuido bajo condiciones de gran señal. En ese mismo año, Ayasli [9] presentó un artículo donde resumía los principios de la amplificación distribuida junto con algunos resultados experimentales. En este artículo, dedicó una sección a la amplificación de potencia donde se resumían los mecanismos que pueden limitar la potencia de una arquitectura clásica de amplificador distribuido. Pronto surgió un problema importante, que estaba relacionado con la baja eficiencia del amplificador distribuido. Hay dos puntos claves que son causa: una contribución desigual a la potencia de salida por parte de los dispositivos activos y la potencia que se pierde en el puerto adaptado de salida. El desarrollo de nuevos estándares de comunicación que cuentan con nuevas, y complejas, modulaciones digitales motivaron una evolución en la etapa amplificadora. Por tanto, los amplificadores distribuidos se retomaron a lo largo de los años [10; 11; 12; 13; 14; 15; 16], con el objetivo de conseguir unas mejores prestaciones en términos de eficiencia y potencia de salida. Sin embargo, en general, un incremento en la potencia de salida conlleva un sacrificio del ancho de banda, por ello es necesario alcanzar un compromiso.

Los primeros intentos que se encuentran en la literatura buscaban un incremento de la ganancia y del ancho de banda empleando un combinador de potencia a la salida que recuperara la potencia que se perdía en el puerto adaptado de salida, y una inyección de potencia simulatánea en los puertos de entrada. Esta idea fue presentada por Aitchison *et. al* en 1988 [13], bajo el nombre de amplificador distribuido *'dual-fed'*, consiguiendo una mejora en la ganancia de 6 dB. Aunque el descubrimiento de esta arquitectura proporcionó un incremento importante de ganancia y una reducción de la figura de ruido a bajas frecuencias, pronto se evidenció que la arquitectura estaba intrínsecamente desadaptada a la entrada. Además, el rápido crecimiento de las aplicaciones de RF requerían un comportamiento paso banda en lugar del paso bajo, que poseía la estructura. En esta línea, Aitchison *et. al* publicaron en 1989 una solución para la desadaptación a la entrada [17], proponiendo un amplificador distribuido *'dual-fed'* en configuración balanceada. Esta solución combina dos amplificadores *'dual-fed'* a través de dos híbridos de 90°. Sin embargo,

esta arquitectura presenta un alto grado de complejidad, lo cual es posiblemente la causa de la ausencia de implementaciones físicas en la literatura. En paralelo, Minnis desarrolló en 1989 [18] una técnica basada en filtros paso banda para conseguir el comportamiento paso banda del amplificador. El objetivo era extender el rango de frecuencia de trabajo, pero desde un punto de vista de pequeña señal sin considerar las condiciones de carga de los dispositivos activos.

En 1994 Campovecchio *et. al* [19] comprendieron que para conseguir que el FET proporcionara potencia a la salida, era esencial considerar las condiciones de carga que necesitaba cada uno de los dispositivos activos. Propusieron un método para conseguir condiciones óptimas de potencia por medio de la modificación de las impedancias características y las longitudes eléctricas de las etapas con objeto de ecualizar las impedancias de carga vistas por cada dispositivo activo. Esta estrategia, en la cual se basa las líneas de drenador en *'taper'* [10; 11; 12], no aprovecha, sin embargo, la potencia que se destina al puerto adaptado de salida. En algunas implementaciones, el puerto adaptado se termina en circuito abierto, reflejando una pequeña porción de la potencia al puerto directo, pero a expensas de un degradación en la adaptación a la salida [11]. Implementaciones de este tipo de amplificadores se han medido proporcionando buenos resultados en términos de eficiencia sobre un ancho de banda considerable, con PAE mayores al 27% sobre un ancho de banda de 2-6 GHz [12].

Un enfoque similar es el adoptado por Narendra *et al.* en [20; 21], donde los dispositivos activos se cargan con valores de impedancia que se obtienen a partir de medidas *'load-pull'*. Estos valores se pueden diseñar ajustando los valores de las fuentes de corriente y los desfases entre etapas. En [21], se han reportado valores de PAE mayores al 30% en un rango de frecuencia de 10-1800 MHz.

La idea del amplificador distribuido *'dual-fed'* [13; 14], fue revivida en 1999 por Eccleston *et. al* con un enfoque de gran señal [22]. Con este enfoque trataron de resolver los dos problemas que se han comentado anteriormente, el uso de la potencia que se pierde en el puerto adaptado y la contribución desigual de los dispositivos activos. Para ello se analizaron las condiciones de carga de cada uno de los dispositivos activos, y se demostró que si se seleccionaban de forma adecuada las longitudes eléctricas y las impedancias características [15], es posible implementar un combinador óptimo de potencia en clase A. Sin embargo, para implementarlo, Eccleston

utilizó líneas de transmisión convencionales para espaciar los FETs 180°, resultando en circuitos de gran tamaño. Además, esta alternativa está intrínsecamente desadaptada, lo cual está mitigado, únicamente, por las pérdidas en la línea de entrada.

La aparición de las líneas de transmisión arficial compuestas diestras-zurdas (CRLH-TLs), como una forma sencilla de implementar líneas con diagramas de dispersión zurdos y diestros [23; 24; 25], abre la puerta a nuevos conceptos en el diseño de los amplificadores distribuidos de potencia. En realidad, se trata de líneas de transmisión artificiales que se basan en una topología de celda unitaria tipo paso banda. De esta manera ofrecen un comportamiento en frecuencia más amplio comparado a las líneas de transmisión diestras convencionales, lo cual ha permitido el desarrollo de nuevos dispositivos de microondas [23; 24].

Los circuitos distribuidos se basan en la propagación a lo largo de una línea de transmisión artificial o continua. Por lo tanto, constituyen un campo interesante donde se puede investigar las aplicaciones potenciales que ofrecen las líneas CRLH. Estas líneas ya se han utilizado en la amplificación distribuida y en etapas de mezclado consiguiendo nuevos diseños que presentan una funcionalidad innovadora tal como el comportamiento doble banda, diplexor ó como rechazo imagen (en el caso de los mezcladores) [26; 27; 28].

Las líneas CRLH han probado su gran potencial y versatilidad ofreciendo nuevas aplicaciones para sistemas conocidos. Esta característica, en sí misma, es razón suficiente para analizar lo que un punto de vista de metamateriales puede ofrecer a la amplificación distribuida de potencia.

E.1.2 Motivación

El escenario descrito anteriormente proporciona una buena perspectiva de la motivación de dicha Tesis Doctoral. En primer lugar, en el campo de la amplificación distribuida de potencia aún queda por resolver los problemas clásicos que presentan dichas estructuras: el uso de la potencia que se pierde en el puerto adaptado y la contribución desigual a la potencia de salida por parte de los dispositivos activos, sin sacrificar la adaptación a la entrada de la estructura. Al mismo tiempo, el rápido desarrollo de nuevas aplicaciones basadas en metamateriales parece motivo suficiente para examinar las oportunidades que esta nueva estructura pudiera aportar a la

amplificación distribuida de potencia.

En este contexto, el desafío consiste en llevar a cabo un estudio exhaustivo del comportamiento intrínseco de un amplificador distribuido genérico en términos de sus condiciones de carga, para poder identificar las opciones de diseño existentes para la implementación un combinador óptimo en Clase A. Siguiendo con dicha idea, parece apropiado investigar si el uso de líneas CRLH podría añadir alguna característica interesante al trabajo que ya se ha llevado a cabo hasta la fecha. Además, se buscarán nuevas topologías que proporcionen un incremento de ganancia sin acarrear una degradación sobre la adaptación a la entrada.

Como en cualquier otro trabajo científico, se buscaran resultados experimentales que corroboren las conclusiones del análisis teórico. Es, por tanto, una tarea de dicha Tesis el diseño, la implementación y medida de prototipos experimentales.

El trabajo no estaría completo sin extender el estudio a clases de trabajo más eficientes, que puedan trabajar con los nuevos esquemas de modulación. Aunque ya se han publicado algunos trabajos en esta línea [29; 30], sería interesante cubrir el problema de una forma más extensa y estructurada.

E.1.3 Contenido de la Tesis

El ***Capítulo 2*** se ha dedicado por completo al estudio del comportamiento intrínsecto, en términos de potencia y ganancia, de un amplificador distribuido discreto. Este capítulo es clave para poder llevar a cabo, con éxito, el diseño de un amplificador distribuido de potencia. Partiendo de un escenario genérico, se desarrollan las fórmulas que permiten predecir las impedancias de carga en el plano intrínseco de los dispositivos activos y, por tanto, su comportamiento en términos de potencia de salida. A partir de dichas fórmulas es posible determinar los casos particulares para los cuales el amplificador trabaja como un combinador óptimo en clase A. Por último, se han considerado los mecanismos que limitan el comportamiento en ganancia y en potencia.

La siguiente tarea consiste en encontrar una solucin a los problemas clásicos de la amplificación distribuida de potencia. En el ***Capítulo 3***, se ha desarrollado un mecanismo de control de ganancia que proporciona condiciones de adaptación perfectas a la entrada. Esta idea está basada en el trabajo publicado por Nguyen *et al.*

[31] y Wu *et al.* [32] para la maximización de la eficiencia en antenas *'leaky-wave'*. En este esquema la potencia no radiada se realimenta en el puerto de entrada en lugar de perderse en una carga adaptada, lo que se conoce como el concepto de *'power recycling'*. El mismo principio se puede aplicar a los amplificadores distribuidos. Esta configuración permite controlar el nivel de ganancia que puede ser, teóricamente, tan grande como se desee manteniendo condiciones de adaptación perfectas en un ancho de banda limitado. El resultado es el llamado amplificador distribuido *'power recycling'*.

El ***Capítulo 4*** constituye la prueba de concepto de los capítulos anteriores. Para ello se ha implementado un prototipo siguiendo la filosofía de diseño publicada en [16], que presenta valores de eficiencia próximos al límite teórico para un amplificador trabajando en clase A en un ancho de banda limitado. La ganancia de este amplificador se puede mejorar realizando algunos ajustes en la línea de puerta. El uso de un divisor de potencia para alimentar de forma simultánea ambas entradas ya ha sido propuesto [13; 14], consiguiéndose incrementos de ganancia del orden de 6dB. El inconveniente de dicha alternativa es la desadaptación intrínseca que presenta, que puede compensarse únicamente gracias a las pérdidas en la línea de puerta. En una segunda versión de dicho prototipo, el problema de la desadaptación a la entrada se soluciona gracias a la configuración *'power recycling'* propuesta. Los resultados experimentales demuestran su viabilidad como combinador óptimo en clase A con incremento de ganancia y valores excelentes de adaptación a la entrada. El capítulo concluye con el diseño de un segundo prototipo en tecnología monolítica.

El trabajo desarrollado en los capítulos anteriores se ha extendido en el ***Capítulo 5*** con el estudio de los amplificadores en modos de alta eficiencia. Este es un paso lógico en el desarrollo del amplificador distribuido *'power recycling'* si se quiere conseguir su mejor rendimiento como amplificador de potencia. Para ello se revisan las condiciones de carga que requieren los amplificadores trabajando en modos de alta eficiencia, y también se evalúan las distintas opciones aplicables a los amplificadores distribuidos de potencia. El capítulo concluye con un diseño de un amplificador de potencia en configuración *'power recycling'* en Clase AB con dispositivos HEMT de GaN.

Finalmente el ***Capítulo 6*** resume los resultados principales y propone líneas de actuación futuras.

E.2 Comportamiento intrínseco de ganancia de los amplificadores distribuidos

El análisis del comportamiento intrínseco del comportamiento de la ganancia de los amplificadores distribuidos se basa en un modelo unilateral, simplificado y sin pérdidas de un dispositivo activo. Los amplificadores distribuidos se basan en el acoplamiento activo de dos líneas de transmisión cargadas periódicamente con dispositivos activos. La topología de un amplificador distribuido uniforme es la que se presenta en la Fig. 2.1. Observe que la línea de transmisión artificial está terminada en su correspondiente impedancia imagen con topología en T, $Z_T(\omega)$ [34].

Una topología particular de amplificador distribuido es la que se muestra en la Fig. 4.6. En este caso se han utilizado celdas unitarias tipo paso banda para conseguir un diagrama de dispersión diestro-zurdo. Los dispositivos activos se modelan mediante un modelo equivalente unilateral y sin pérdidas consistente en un generador de corriente controlado por tensión y dos capacidades (de entrada y de salida, ver Fig. 2.2), que son absorbidas por las celdas unitarias.

Un amplificador distribuido es un dispositivo de cuatro puertos, aunque normalmente tan sólo se usan dos de ellos como puertos de entrada y de salida, mientras que los otros dos quedan cargados con su impedancia, imagen o característica, de las correspondientes celdas unitarias. Por tanto, es posible definir dos ganancias diferentes en el amplificador distribuido: la directa (entre los puertos 1 y 4) y la inversa (entre los puertos 1 y 3) (ver Fig. 2.1).

Se puede demostrar [34] que las ganancias vienen dadas por las siguientes expresiones:

$$G_{forward} = \frac{g_m^2 \Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}}{4} \frac{|Z_{\pi d}(\omega)||Z_{\pi g}(\omega)|}{|Z_{Td}(\omega)||Z_{Tg}(\omega)|} \left| \frac{\sin\left[\frac{N}{2}(\theta_d(\omega) - \theta_g(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_d(\omega) - \theta_g(\omega))\right]} \right|^2 \tag{E.1}$$

$$G_{reverse} = \frac{g_m^2 \Re\{Z_{Td}(\omega)\}\Re\{Z_{Tg}(\omega)\}}{4} \frac{|Z_{\pi d}(\omega)||Z_{\pi g}(\omega)|}{|Z_{Td}(\omega)||Z_{Tg}(\omega)|} \left| \frac{\sin\left[\frac{N}{2}(\theta_d(\omega)+\theta_g(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_d(\omega)+\theta_g(\omega))\right]} \right|^2 \quad \text{(E.2)}$$

Cabe resaltar que, aparte de la dependencia con la frecuencia asociada a las impedancias imagen de las celdas unitarias con topología en π y en T, $Z_{\pi g}(\omega)$, $Z_{\pi d}(\omega)$, $Z_{Tg}(\omega)$ y $Z_{Td}(\omega)$, la respuesta en frecuencia de ambas ganancias está controlada por los desfases de las celdas unitarias, $\theta_d(\omega)$ y $\theta_g(\omega)$, la transconductancia, g_m, y el número total de dispositivos activos, N. También es importante señalar que la ganancia directa está controlada por la diferencia entre los desfases, mientras que la ganancia inversa depende de la suma de los desfases.

En un amplificador distribuido convencional, se utilizan celdas tipo paso bajo (ó líneas de transmisión diestras) con la condición $\theta_d(\omega) = \theta_g(\omega)$, lo cual resulta en un comportamiento de banda ancha para la ganancia directa (limitado por las frecuencias de corte de las celdas unitarias), y en un comportamiento paso bajo con ancho de banda limitado para la ganancia inversa. Como resultado se produce un máximo en la ganancia directa en todo el rango de frecuencia hasta la frecuencia de corte, y un máximo en la ganancia inversa a $f = 0$. Esta es la razón por la cual tan sólo se utilizan los puertos 1 y 4 cuando se persigue una amplificación de banda ancha. Sin embargo, nuevas opciones de diseño aparecen si se utiliza un diagrama de dispersión en frecuencia más rico a través del uso de celdas CRLH [28].

E.3 Comportamiento intrínseco de potencia de los amplificadores distribuidos

El esquema de amplificador distribuido que se muestra en la Fig. 2.1 también se puede utilizar para evaluar su comportamiento intrínseco de potencia. Bajo las simplificaciones que se han asumido anteriormente, tanto en la estructura de amplificador distribuido como en el circuito equivalente del dispositivo activo, la potencia que proporciona cada uno de los dispositivos activos está controlada por

la impedancia de carga en su plano de referencia. Por tanto, estas impedancias de carga (Z_{Lk}) son un factor clave en la discusión sobre el comportamiento intrínseco de potencia de los amplificadores distribuidos.

Utilizando el principio de superposición, la tensión en el plano intrínseco de salida del dispositivo k se puede calcular con facilidad, cuyo resultado es

$$V_k = \sum_{l=1}^{N} V_k^l = Z_{\pi d}(\omega)\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\sum_{l=1}^{N}\frac{I_{indl}}{2}e^{-j\theta_d(\omega)|k-l|} \tag{E.3}$$

Teniendo en cuenta que la impedancia de carga, Z_{Lk}, en el plano intrínseco del dispositivo k está definido por

$$Z_{Lk}(\omega) = \frac{V_k}{I_{indk}} \tag{E.4}$$

se pueden obtener las siguientes ecuaciones:

- If $k \leq \frac{N}{2}$, N-even or $k \leq \frac{N+1}{2}$, N-odd

$$\begin{aligned} Z_{Lk}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\Bigg[& e^{j(\theta_g(\omega)-\theta_d(\omega))\frac{k}{2}}\frac{\sin\left[\frac{(k-1)}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]} \\ & + e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(N-k)}{2}}\frac{\sin\left[\frac{(N+1-k)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\Bigg] \end{aligned} \tag{E.5}$$

- If $k > \frac{N}{2}$, N-even or $k > \frac{N+1}{2}$, N-odd

$$\begin{aligned} Z_{Lk}(\omega) = \frac{Z_{\pi d}(\omega)}{2}\sqrt{\frac{Z_{\pi d}(\omega)}{Z_{Td}(\omega)}}\Bigg[& e^{-j(\theta_g(\omega)-\theta_d(\omega))\frac{(1-k)}{2}}\frac{\sin\left[\frac{k}{2}(\theta_g(\omega)-\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)-\theta_d(\omega))\right]} \\ & + e^{-j(\theta_g(\omega)+\theta_d(\omega))\frac{(N-k+1)}{2}}\frac{\sin\left[\frac{(N-k)}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}{\sin\left[\frac{1}{2}(\theta_g(\omega)+\theta_d(\omega))\right]}\Bigg] \end{aligned} \tag{E.6}$$

Estas dos ecuaciones muestran que, en general, las impedancias de carga de cada dispositivo activo para una determinada frecuencia es diferente y, por tanto, contribuirán con diferentes niveles de potencia a la salida del amplificador distribuido. Para conseguir condiciones óptimas de potencia a la salida es necesario que la impedancia de carga vista por cada dispositivo sea real e igual a su valor óptimo (Fig. 2.8). Este valor óptimo viene dado por la siguiente expresión (clase A) [36]

$$R_{Lopt} = V_{dc}/(I_{max}/2) = V_{dc}/I_{dc} \tag{E.7}$$

con la condición de que el dispositivo esté polarizado en el siguiente punto

$$I_{dc} = \frac{I_{max}}{2}, V_{dc} = \frac{V_{max}}{2} \tag{E.8}$$

Además, a partir de las ecuaciones (E.5) y (E.6) se puede demostrar con facilidad que la impedancia de carga Z_{Lk} adquiere un valor real que viene dado por

$$Z_{Lk} = \frac{N}{2} Z_{\pi d} \sqrt{\frac{Z_{\pi d}}{Z_{Td}}} \tag{E.9}$$

cuando $\theta_g = \theta_d = \pm m\pi$ ó cuando $\theta_g = -\theta_d = \pm m\pi$, siendo m un valor entero (m=0,1,2,...). Esta expresión se puede reducir simplemente a

$$Z_{Lk} = \frac{N}{2} Z_{\pi d} \tag{E.10}$$

para los valores de desfase en los cuales $Z_{\pi d} = Z_{Td}$.

Esto significa que, bajo cualquiera de estas condiciones, cada dispositivo activo contribuye con el mismo nivel de potencia a la salida del amplificador. Si las celdas unitarias se diseñan de acuerdo a la ecuación (E.10), con objeto de proporcionar la impedancia carga real y óptima que requiere cada uno de los dispositivos, se consigue la máxima potencia a la salida del amplificador. Estos resultados concuerdan con aquellos conseguidos previamente por Eccleston [15].

Como ejemplo, consideremos un amplificador distribuido de cinco etapas. La potencia normalizada (con respecto a su máximo valor) que proporciona el tercer dispositivo en función de los desfases de puerta y drenador está representado en la Fig. 2.9. A partir de esta figura es evidente cuales son los valores óptimos para

θ_g y θ_d. Tenga en cuenta que tanto los valores del desfase entre etapas positivos como los negativos se han tenido en cuenta puesto que es posible obtener ambos con las celdas CRLH. Los valores de desfase cero son de un interés particular ya que se pueden implementar a una frecuencia arbitraria utilizando celdas unitarias CRLH tipo paso banda. Su uso ya fue propuesto por Eccleston [37] para acortar el tamaño del amplificador distribuido, así como para incrementar su ancho de banda.

La influencia de los desfases en puerta y en drenador sobre las ganancias directa e inversa se han representado en las Figs. 2.10 y 2.11, respectivamente, para un amplificador distribuido de cinco etapas. Se puede apreciar en estas figuras que el máximo valor para la ganancia directa se obtiene cuando $\theta_g(\omega) = \theta_d(\omega)$, y cuando $\theta_g(\omega) = -\theta_d(\omega)$ para la ganancia inversa. Esto significa que a través de un diseño adecuado de los desfases en puerta y drenador es posible obtener la máxima potencia de salida de cada uno de los dispositivos activos y valores máximos en ambas ganancias (directa e inversa) a una determinada frecuencia.

E.4 Teoría de operación: amplificador distribuido en configuración *'power recycling'*

En esta sección se presenta el principio de funcionamiento del amplificador distribuido en configuración *'power recycling'*. Dicha arquitectura combina la característica de máxima transferencia de potencia derivada de un diseño adecuado del desfase de las celdas unitarias junto con el incremento de ganancia que proporciona el uso de un esquema de reciclado de potencia [31; 32] en la línea de transmisión en puerta. La arquitectura básica del PRDA se detalla en la Fig. 3.1. Se basa en el diseño de los amplificadores distribuidos para máxima potencia. Un combinador recoge la potencia de salida de los puertos directo e inverso, mientras que la línea de puerta se realimenta gracias a un acoplador direccional (simétrico ó antisimétrico) y dos tramos de línea de transmisión adicionales (Z_0, θ_{aux1} and θ_{aux2}).

En resumen, la potencia que se inyecta en el puerto 6 se divide, derivando una parte al puerto 5, y por tanto a la línea de puerta del amplificador distribuido, y derivando otra parte al puerto adaptado (puerto 8). La inyección de dicha onda

de potencia, b_5, a la línea de puerta genera otra onda, a_7, que vuelve a inyectarse en el acoplador direccional. De nuevo, para de esta energía termina en el puerto adaptado, mientras que el resto contribuye a incrementar la energía de la onda b_5, si se selecciona un correcto desfase en la línea auxiliar.

A través de un diseño apropiado, este innovador amplificador distribuido puede proporcionar máxima potencia a la salida, y al mismo tiempo, condiciones de adaptación perfectas a la entrada junto con un control o incremento de ganancia.

E.4.1 Comportamiento intrínseco

Para discutir el comportamiento intrínseco del PRDA, esto es, el mejor comportamiento que se puede conseguir en condiciones ideales, se ha llevado a cabo un análisis simplificado. El análisis se basa en la idea propuesta por Nguyen *et. al* [31] para la maximización de la eficiencia de las antenas *'leaky wave'*. En aras de la integridad, algunos resultados publicados en [31] se han reproducido en esta subsección. El amplificador distribuido se considera unilateral y la línea de puerta se modela como una línea de transmisión sin pérdidas de impedancia característica Z_0 y longitud eléctrica θ_{g_line}. Los tramos de línea de transmisión adicionales también tienen impedancia característica Z_0 y son sin pérdidas (θ_{aux1} and θ_{aux2}). El acoplador direccional también es ideal y sin pérdidas con una respuesta antisimétrica (la respuesta simétrica se discutirá más adelante). Bajo estas simplificaciones, y teniendo en cuenta que la matriz de parámetros S de un acoplador direccional ideal y sin pérdidas viene dada por [39]

$$[S] = -j \begin{bmatrix} 0 & A & B & 0 \\ A & 0 & 0 & -B \\ B & 0 & 0 & A \\ 0 & -B & A & 0 \end{bmatrix}, A^2 + B^2 = 1; A, B \in \mathbb{R} \tag{E.11}$$

Es inmediato obtener el valor de la onda de potencia de entrada al puerto 5, esto es [40]

$$b_5 = \frac{-jA \cdot a_6}{1 + jB \cdot e^{-j(\theta_{g\_line} + \theta_{aux1} + \theta_{aux2})}} \tag{E.12}$$

y también, que $a_5 = b_6 = b_7 = 0$. $b_8 = 0$, lo cual significa que la estructura presenta condiciones de adaptación perfectas, mientras que $a_5 = b_7 = 0$ indica que tan sólo hay una onda propagándose a través de la línea de puerta desde el puerto 5 al puerto 7. Por tanto, la ganancia completa del amplificador está gobernada por el cociente b_5/a_6. La ecuación (E.12) claramente indica que este cociente es, para un valor cualquiera de acoplamiento, máximo si [31]

$$e^{-j(\theta_{g\_line}+\theta_{aux1}+\theta_{aux2})} = j \tag{E.13}$$

esto es [40],

$$\theta_{g\_line} + \theta_{aux1} + \theta_{aux2} = \frac{3\pi}{2} + 2\pi m \tag{E.14}$$

siendo m un entero, y significa que la ganancia está controlada por el factor de acoplamiento del acoplador direccional. El incremento de ganancia en función del factor de acoplamiento, A, se muestra en la Fig. 3.2. Por ejemplo, si se usa un acoplador direccional de 3dB, el máximo valor para el cociente b_5/a_6 es 2.42, lo cual representa un incremento de 7.6 dB en la ganancia completa del amplificador, a lo cual hay que sumar 3dB correspondientes a la combinación de potencia en los puertos de salida. Por tanto, se consigue un incremento de 10.6 dB al compararlo con la ganancia de un amplificador distribuido en configuración *'single-fed'* (inyección de potencia en el puerto 1, y puerto 2 terminado con su carga adaptada).

El incremento de la ganancia puede ser tan alto como se desee, Fig. 3.2, por medio de un grado de acoplamiento extremadamente bajo entre los puertos 5 y 6, $A \to 0$, que constituye una limitación desde el punto de vista de la implementación. Si $A = 1$, no hay acoplamiento entre los puertos 5 y 7, lo cual corresponde a un alimentación *'single-fed'*. En este caso, los 3 dB de incremento de ganancia que aparecen en la Fig. 3.2 se deben, por tanto, a la combinación de potencia de los puertos 3 y 4.

Si consideramos un acoplador direccional simétrico, ideal y sin pérdidas (ver Fig. 3.3), en lugar de un antisimétrico, se obtienen resultados similares. Considerando que la matriz de parámetros S viene dada por [39]

$$[S] = -j \begin{bmatrix} 0 & A & -jB & 0 \\ A & 0 & 0 & -jB \\ -jB & 0 & 0 & A \\ 0 & -jB & A & 0 \end{bmatrix}, \quad \begin{matrix} A^2 + B^2 = 1 \\ A, B \in \mathbb{R} \end{matrix} \tag{E.15}$$

La condición para máxima ganancia se puede calcular, y viene dada por [40]

$$\theta_g + \theta_{aux1} + \theta_{aux2} = \pi + 2\pi m \tag{E.16}$$

siendo m un número entero. Los niveles de ganancia que se pueden conseguir son idénticos a aquellos que proporciona el acoplador direccional antisimétrico.

Dos características son, principalmente, las responsables de la degradación del comportamiento intrínseco del amplificador: las pérdidas y la desadaptación. Ambas establecen un límite a la máxima ganancia que se puede conseguir y a los valores de adaptación. Su efecto se ha evaluado en la siguiente subsección.

E.4.2 Efecto de la desadaptación y de las pérdidas

El comportamiento intrínseco del amplificador propuesto está afectado, principalmente, por la desadaptación y por las pérdidas relacionadas con la línea de transmisión de puerta del amplificador distribuido de 4 puertos.

En primer lugar, se analizarán el impacto de las pérdidas. Para ello, la línea de puerta tiene condiciones de adaptación perfectas pero se introduce un factor de atenuación $\alpha_{g\_line}L$. El conjunto de parámetros S que definen la línea de transmisión de puerta viene dado ahora por $S_{11} = S_{22} = 0$ y $S_{21} = S_{12} = e^{-(\alpha_{g\_line}L + j\theta_{g\_line})}$. Si se consideran las pérdidas, la ganancia no puede crecer indefinidamente, sino que alcazará un máximo valor que se puede obtener al maximizar la magnitud b_5/a_6. El resultado indica que el máximo valor de la ganancia se alcanza si se imponen las condiciones de fase (E.14) ó (E.16) para los casos anti- y simétrico, respectivamente. En ambos casos el amplificador mantiene unas condiciones de adaptación perfectas y existe un valor para el grado de acoplamiento, A, que garantiza un máximo de ganancia, el cual viene dado por [31]

$$A = \sqrt{1 - e^{-2\alpha_{g\_line}L}} \tag{E.17}$$

Para evaluar el impacto de la desadaptación, asumimos que la línea de puerta del amplificador distribuido tiene una impedancia característica real, Z_g, diferente de Z_0, y una constante de atenuación $\alpha_{g\_line}L$. Por tanto, se debe definir una nueva matriz de parámetros S para la línea de transmisión de puerta (ver el Apéndice B).

El análisis de la estructura que se muestra en la Fig. 3.1 da como resultado el valor del coeficiente de reflexión a la entrada, b_6/a_6, cuando se alcanza la condición de fase óptima (E.14) ó (E.16). La adaptación a la entrada es ahora, obviamente, dependiente de los parámetros Γ y $\alpha_{g\_line}L$. La magnitud del coeficiente de reflexión a la entrada en función de Γ, con $\alpha_{g\_line}L$ como parámero se muestra en la Fig. 3.4 para un valor particular de acoplamiento ($A = 1/\sqrt{2}$) (ver el Apéndice B). A partir de esta figura, se puede deducir con facilidad que existe un límite para la desadaptación y las pérdidas en la puerta que se puede tolerar si se busca un determinado valor de adaptación a la entrada. El efecto de la desadaptación y las pérdidas en la puerta sobre el incremento en la ganancia en potencia se puede observar en la Fig. 3.5 para el mismo valor de acoplamiento ($A = 1/\sqrt{2}$) (ver el Apéndice B). Como se esperaba, la ganancia en potencia decrece al aumentar las pérdidas. Se puede ver en esta figura que las pérdidas en la línea de puerta tienen un mayor impacto sobre la ganancia del amplificador que la desadaptación en puerta.

Aunque las Figs. 3.4 y 3.5 se han calculado para un acoplador direccional de 3dB, la misma información se puede extraer para cualquier grado de acoplamiento (ver el Apéndice B). Vale la pena mencionar que incluso en presencia de la desadaptación y de las pérdidas en la puerta, el incremento en el nivel de ganancia puede ser arbitrario, hasta un valor máximo determinado por la ecuación (E.17), decrementando el factor de acoplamiento, A. Sin embargo, la adaptación a la entrada del amplificador se hace más sensible al parámetro Γ a medida que A crece, lo cual impone una limitación práctica a los valores de ganancia y adaptación a la entrada que se pueden conseguir. A pesar de ello, este hecho no evita la posibilidad de implementar este nuevo concepto de amplificador si se lleva a cabo un diseño adecuado.

E.5 Prototipo experimental: amplificador distribuido paso banda de 3 etapas en configuración *'power recycling'*

Para validar la teoría de las secciones anteriores, se ha construido y medido un prototipo experimental de un amplificador distribuido de tres etapas con dispositivos pHEMT, basado en celdas unitarias CRLH. Los resultados experimentales corroboran las conclusiones principales que se derivan del análisis simplificado. Estos resultados, que ya han sido publicados en [16] y en [40], son la primera referencia en la literatura, hasta donde saben los autores, de un prototipo de amplificador distribuido diseñado con celdas CRLH y desfase de $\theta = 0$ a la frecuencia de trabajo. La teoría descrita en [16], ha sido adoptada recientemente por los autores Fei et al. [41] para la implementación de un amplificador de potencia 2-D para la banda de 60 GHz en tecnología CMOS de 65 nm, lo cual prueba la viabilidad del diseño de un amplificador de potencia distribuido inspirado en metamateriales para distintos procesos tecnológicos.

Se ha construido y medido un amplificador distribuido de tres etapas en configuración *'power recycling'*. Para ello se ha elegido un dispositivo activo p-HEMT (ATF-35143). El punto de trabajo sugerido para trabajar en clase-A es $I_{DS} = 30mA$, $V_{DS} = 3.0V$, y la resistencia de carga óptima estimada en el plano intrínseco es de 75Ω. Fijando la resistencia de carga óptima y el número de etapas, se puede utilizar la ecuación (E.10) para obtener la impedancia característica de la línea de drenador: 50Ω. Este resultado permite sintetizar una impedancia de 50Ω tanto para la línea de drenador como para la de puerta.

Para reducir el tamaño del circuito, se han utilizado líneas de transmisión CRLH (Fig. 4.6). Tanto las celdas unitarias de puerta como las de drenador son idénticas, y se han diseñado para presentar un desfase de valor cero ($\theta_g = \theta_d = 0$) a la frecuencia de trabajo de 1 GHz. Esta condición hace que los tres dispositivos trabajen con las mismas condiciones de carga y, por tanto, que suministren la misma potencia a la salida. La implementación se ha llevado a cabo en un sustrato FR-4 utilizando componentes concentrados 0603. Las capacidades de entrada y de salida, C_{gs} y

C_{ds}, de los dispositivos activos se han absorbido en las celdas unitarias CRLH. Los valores de los componentes comerciales para los componentes concentrados se han resumido en la Tabla E.1. El amplificador que se ha fabricado se muestra en la Fig. 4.7.

Table E.1: Valores comerciales para los componentes concentrados de la línea de transmisión CRLH

$C_{R_{gaux}}$	$C_{R_{daux}}$	$L_{R_{g/d}}$	$C_{L_{g/d}}$	$L_{L_{g/d}}$
0.9pF	1.6pF	5.1nH	2.7pF	4.3nH

En primer lugar, el amplificador distribuido de cuatro puertos, Fig. 4.7, se ha caracterizado en régimen de pequeña señal. Las ganancias de potencia y el coeficiente de reflexión a la entrada (en magnitud) se han medido y simulado, como se muestra en la Fig. 4.8. Se observa una concordancia razonable entre la simulación y las medidas. Los buenos valores de adaptación a la entrada que se han conseguido a la frecuencia de diseño de 1 GHz es una condición necesaria para abordar con éxito la implementación de un PRDA. Observe que hay un desplazamiento de 70 MHz en la frecuencia medida a la cual la adaptación a la entrada presenta su mejor comportamiento. Estas discrepancias entre las simulaciones y las medidas se podrían explicar, principalmente, debido al uso de los parámetros S que proporciona el fabricante para los dispositivos activos, y también a las tolerancias de los valores de los componentes pasivos y activos.

Por razones ilustrativas se ha elegido un acoplador direccional de 3dB. Por tanto, el amplificador en configuración *'power recycling'* se ha construido añadiendo externamente dos híbridos de 180° tanto a los puertos de entrada como de salida del prototipo que se muestra en la Fig. 4.7, de acuerdo al esquema que se puede observar en la Fig. 3.1. Observe que este valor concreto de acoplamiento no proporciona el máximo incremento de ganancia. Dos desfasadores externos (JSPHS-1000) se han añadido a los conectores de los puertos 1 y 3 para alcanzar las condiciones de fase requeridas (E.14). Para estas medidas no se han descontado las pérdidas relativas a los combinadores externos, ni las de los conectores físicos, pero sí se han descontado las pérdidas derivadas de los desfasadores externos. El coeficiente de reflexión a la entrada y la ganancia en potencia medida y simulada de este prototipo se muestran

en la Fig. 4.9. La máxima ganancia se alcanza para la frecuencia a la cual el amplificador distribuido de 4 puertos consigue sus mejores niveles de adapación, 1.07 GHz. El incremento de ganancia medido a dicha frecuencia es de 6 dB comparado con la configuración *'single-fed'*, lo cual está cerca del valor teórico (entre 7.4 y 7.7 dB), que se obtiene a partir del análisis simplificado de la sección anterior (Fig. 3.5) para los siguientes valores: $\alpha_{g\_line}L = 0.19$ y $|\Gamma| = 0.05$ (valores medidos). El coeficiente de reflexión a la entrada es mejor de 27 dB a la frecuencia de trabajo. Estos dos resultados, el incremento de ganancia de 6 dB y el coeficiente de reflexión a la entrada de 27 dB demuestran la viabilidad de la arquitectura de amplificador propuesta.

Puesto que el prototipo se ha construido añadiendo híbridos externos al amplificador distribuido básico de la Fig. 4.7, es posible comparar el comportamiento experimental de las tres configuraciones posibles: *'single-fed'*, *'dual-fed'*, y *'power recycling'*. El comportamiento en régimen de pequeña señal de estos tres amplificadores se muestra en la Fig. 4.10. Vale la pena remarcar que el valor más alto de ganancia que presenta buenos niveles de adaptación corresponde al amplificador distribuido en configuración *'power recycling'*.

La potencia de salida en el punto de compresión de 1dB que proporciona el fabricante para un único dispositivo, en el punto de polarización elegido, es alrededor de 14dBm. Si tres dispositivos activos se combinaran de forma perfecta, el valor esperado para el punto de compresión sería de 14dBm + 4.8 dB = 18.8 dBm. La potencia de salida medida en dicho punto para el prototipo de tres etapas es de 18 dBm (Fig. 4.11), y la PAE del amplificador a la frecuencia de 1.07 GHz está alrededor del 27% para el punto de compresión de 1 dB, lo cual sugiere que los tres dispositivos están trabajando bajo condiciones similares y próximas a las óptimas para clase A.

Para evaluar la linealidad exhibida por la configuración *'power recycling'*, el IMD se ha medido y comparado con el amplificador en configuración *'single-fed'* que se publicó en [16]. Se espera que el comportamiento en distorsión sea idéntico, puesto que se han utilizado los mismos dispositivos activos y la frecuencia de trabajo también es la misma en ambos prototipos. En la Fig. 4.12 se han superpuesto ambas respuestas. Observe que el eje de potencia de entrada se debe desplazar para poder proporcionar una comparación justa, que debe referenciarse al nivel de potencia de

salida. Estos resultados evidencian que en la configuración *'power recycling'* no se sacrifica linealidad para conseguir un incremento en la ganancia.

También se han llevado a cabo medidas con señales moduladas, que se han realizado con ayuda del software 89600 VSA de Agilent, lo cual proporciona una idea de la linealidad del amplificador cuando trabaja con esquemas de modulación más complejos. Las Figs. 4.13, 4.14 and 4.15 muestran la respuestas para una señal 4FSK, EDGE, y GSM, respectivamente, para el punto de compresión de 1dB. Todas las medidas muestran una buena linealidad, con valores de EVM por debajo del 1% en todos los casos.

Resumiendo, la comparación en régimen de gran señal con las configuraciones *'single-fed'* y *'dual-fed'* muestran que el amplificador distribuido en configuración *'power recycling'* es la única implementación que puede combinar de forma óptima la potencia de salida de un número arbitrario de dispositivos activos con buenos valores de adaptación a la entrada combinado con un nivel de ganancia arbitrario. Por tanto, se sacrifica ancho de banda por un incremento en la ganancia y en la potencia de salida. Esto podría ser interesante en rangos de frecuencia elevados donde la potencia disponible es muy baja, y por tanto podría competir con otras técnicas para la combinación de potencia. Sin embargo, dado que el trabajo en rangos más elevados de frecuencia viene acompañado de un incremento de coste, pérdidas y problemas de acoplamiento entre elementos, la tecnología MMIC es práctivamente un requisito. Recientemente, Fei *et al.* [41] han presentado un amplificador de potencia para 60 GHz en tecnología de 65nm basado en líneas de transmisión CRLH con desfase cero. En este trabajo los autores resaltan los problemas más importantes asociados a la subida en frecuencia. Como mencionan, para este rango de frecuencia, las líneas CRLH no se pueden considerar ideales debido a los altos valores de los elementos parásitos de los transistores, por tanto, las pérdidas y los errores de fase se deben considerar con cuidado para prevenir una degradación importante en el comportamiento del amplificador. El análisis muestra que a medida que el número de etapas aumenta, la degradación de la ganancia en potencia también se incrementa, así que tanto las pérdidas como el error de fase limitan el número máximo de etapas que se pueden implementar. Por otro lado, en el rango de frecuencias de las milimétricas, las capacidades y los inductores concentrados que se necesitan para construir la línea CRLH son más compactos y tienen menos pérdidas, lo cual hace

posible que la implementación *'on-chip'* sea posible. Además, al utilizar dispositivos sin encapsular, se puede diseñar la periferia de los transistores, lo cual puede ser de utilidad a la hora de alcanzar los requisitos de carga que imponen los valores que impedancia característica que se pueden sintetizar en las líneas de transmsión artificiales.

E.6 Amplificadores distribuidos de potencia trabajando en modos de alta eficiencia

El comportamiento en régimen de gran señal de cualquier dispositivo activo está determinado no sólo por su impedancia de carga correspondiente a la frecuencia de trabajo, sino también por la impedancia de carga que ve a los distintos armónicos. Estos valores son fundamentales para el diseño de amplificadores de potencia en modos de alta eficiencia.

El diseño de los amplificadores distribuidos, por otro lado, está basado en la síntesis de líneas de transmisión artificiales. Este proceso determina la carga tanto al fundamental como a los distintos armómicos de frecuencia. Para evaluar la capacidad de los amplificadores distribuidos en el conformado de los distintos armónicos, se han presentado expresiones genéricas para la impedancia de carga en el plano intrínseco para los dispositivos activos que componen un amplificador distribuido (ver la sección E.3).

En las Figs. 5.13 y 5.14, se presentan las impedancias de carga para un amplificador distribuido de cinco etapas en configuración *'single-fed'* basados en líneas CRLH y RH, respectivamente. Se puede observar que la parte real (en línea continua) de los cinco dispositivos activos es dependiente de la frecuencia y diferente para cada unos de los dispositivos, pero alcanza el mismo valor, $\frac{N}{2}Z_{0d}$ (ver la sección E.3), para un conjunto de valores discretos de las constantes de fase, como por ejemplo, $\theta_g = \theta_d = 0$ ó $\theta_g = \theta_d = \pi$. Para estos desfases, la parte real de la impedancia de carga de los cinco dispositivos son coincidentes y la parte imaginaria vale cero. Más allá de las frecuencias de corte, sin embargo, las impedancias de carga se vuelven púramente imaginarias (líneas discontinuas). Se puede observar que el

comportamiento de dichas impedancias de carga está gobernado por la respuesta en frecuencia de la impedancia imagen con topología en π (Figs. 5.15 y 5.16). En ellas se aprecia que la impedancia de carga está próxima a un circuito abierto cerca de las frecuencias de corte y tiende al cortocircuito para los armónicos de alta frecuencia.

Opciones de diseño. Nos centraremos de nuevo en la Fig. 5.13 para discutir las posibilidades de diseño de los amplificadores distribuidos trabajando como amplificadores de potencia. En la sección 5.2, se llevó a cabo una revisión del diseño de amplificadores en modos de alta eficiencia. A continuación se discutirá la validez de dichos efoques en una configuración de amplificador distribuido.

1. *Configuración en Clase E:* para que el dispositivo activo trabaje como un interruptor, se deben cumplir condiciones de voltaje cero y derivada del votaje cero. El análisis de la carga a la frecuencia del fundamental, una vez impuestas estas dos condiciones, da como resultado la ecuación (5.26) en el plano intrínseco. La evaluación de dicha expresión nos dice que, en general, la carga a la frecuencia del fundamental en el plano intrínseco de los dispositivos activos será un valor complejo. Para conseguir una contribución idéntica a la potencia de salida en un amplificador distribuido, las impedancias de carga de todos los dispositivos activos debe ser idéntica. Se ha demostrado que este fenómeno tan sólo se da a frecuencias singulares e impone una impedancia real para todos los dispositivos. Por tanto, la configuración en Clase E no es una opción implementable en una configuración de amplificador distribuido.

2. *Configuración en Clase F:* la configuración en Clase F requiere que la impedancia a la frecuencia fundamental sea real en el plano intrínseco y que se lleve a cabo un conformado adecuado de los armónicos para conseguir que la forma de onda en tensión/corriente sea una onda cuadrada. La primera condición se puede cumplir en un amplificador distribuido como se ha visto en la sección E.3, garantizando así una contribución idéntica por parte de todos los dispositivos activos. El conformado multi-armónico es, por otro lado, una condición más complicada de cumplir. El amplificador de potencia ideal en Clase F requiere sintetizar un circuito abierto en los armónicos impares y un corto circuito en los armónicos pares (Clase F), ó la síntesis de un corto circuito en los

armónicos impares y un circuito abierto en los pares (Clase F^{-1}). Volviendo a la Fig. 5.13, se puede apreciar que el enfoque más lógico es la síntesis de un amplificador en Clase F^{-1} de orden finito, puesto que el comportamiento natural de la impedancia imagen con topología en π (Fig. 5.15) impone un circuito abierto a la frecuencia de corte y tiende a un corto circuito para altas frecuencias.

Sin embargo, si la impedancia de carga en drenador adquiere un valor real constante, como por ejemplo 50Ω, en lugar de su impedancia imagen, las impedancias de carga en el plano intrínseco adquieren los valores que se observan en la Fig. 5.17. En esta figura se puede apreciar que no se alcanza un circuito abierto. Para solventar este problema, otros autores [30] han introducido una red multi-armónica en el puerto de salida, consiguiendo medidas de eficiencia en drenador del 71%.

3. *Modos convencionales de alta eficiencia:* la teoría de diseño clásida busca una sinusoide pura como la forma de onda de la tensión a la salida. Para ello, la frecuencia fundamental debe cargarse con un valor resistivo puro mientras que los armónicos se terminan en corto circuito. Por tanto, cualquiera de estos modos, por ejemplo, la Clase A, AB, B ó C, es susceptible de ser implementada en un amplificador distribuido. Por supuesto, se necesitan aplicar unas condiciones de polarización adecuadas y diseñar las líneas de transmisión para absorber correctamente las capacidades de entrada y de salida de los dispositivos activos. Puesto que las impedancias de carga de los dispositivos activos tienden al corto circuito si la frecuencia está lo suficientemente alejada de la banda de paso (Fig. 5.13), para conseguir un corto circuito, las frecuencias de corte de la estructura tendrán que elegirse de forma adecuada para que el corto circuito aparezca antes del segundo armónico.

   Para ilustrar la teoría, se han llevado a cabo tres simulaciones diferentes en clase A, AB y B, utilizando un modelo de FET cúbico de Curtice no lineal. Se ha diseñado una banda de paso estrecha, de modo que la frecuencia de corte esté próxima a la frecuencia fundamental y los armónicos se puedan considerar un corto circuito (Fig. 5.17). Las Figs. 5.18 , 5.19 y 5.20 muestran las formas de onda de salida y la PAE para un amplificador distribuido de tres etapas

basado en líneas CRLH trabajando en Clase A, AB y B, respectivamente. La Fig. 5.21 muestra las impedancias de carga para los tres dispositivos activos funcionando en clases de trabajo diferentes. Las líneas de transmisión artificiales se han diseñado para que presenten desfase cero a la frecuencia de trabajo, f_0. Se puede observar a partir de estas figuras que las formas de onda de salida y la PAE están próximas a los valores ideales (Fig. 5.1). Además, a f_0, el desfase entre etapas se ha elegido para que sea cero, de forma que las rectas de carga y las formas de onda sean idénticas para los tres dispositivos activos. Por tanto, bajo una selección correcta del punto de polarización y un diseño adecuado de las líneas de transmisión artificiales es posible conseguir un combinador óptimo de potencia en Clase A, AB, B ó C.

E.7 Conclusiones

Esta tesis doctoral se propuso para investigar nuevas ideas, inspiradas en metamateriales, que pudieran aportar alternativas al campo de amplificación de potencia distribuida. En este último apartado se repasan las contribuiciones más importantes que se han extraido de esta Tesis, así como líneas futuras de actuación.

Contribuciones

El ***Capítulo 2*** constituye las bases en las cuales se sustenta el resto del trabajo realizado. En él se lleva a cabo una revisión del análisis en pequeña señal de los amplificadores distribuidos, para proporcionar una visión completa del problema a los lectores, y se lleva a cabo un estudio exhaustivo del comportamiento intrínseco de potencia de los amplificadores distribuidos uniformes. Para ello, se han estudiado las condiciones de carga que presentan los dispositivos activos en un amplificador distribuido genérico. Este análisis se puede consideran como una de las contribuciones más importantes de esta Tesis, puesto que sienta las bases para el estudio de cualquier estructura distribuida de potencia. Los resultados obtenidos confirman la existencia de un conjunto discreto de condiciones de fase, que deben cumplir las líneas de transmisión artificial, que permiten que todos los transistores trabajen bajo

las mismas condiciones, reales, de impendacia de carga. Bajo estas condiciones el amplificador distribuido puede trabajar, por tanto, como un combinador de potencia óptimo en clase A. Dicho anális también pone de manifiesto que el uso de las líneas de transmisión CRLH se puede aprovechar para conseguir un comportamiento paso-banda que permite una reducción en el tamaño del circuito. Los resultado obtenidos se han extendido con el estudio de una estructura que presenta una inyección simultánea de potencia, conocida como amplificador distribuido *'dual-fed'*, con resultados similares.

En el ***Capítulo 3*** se presenta una solución a un problema sin respuesta en la literatura. Se ha propuesto y analizado una arquitectura novedosa que resuelve los dos problemas principales que aparecen los amplificadores distribuidos de potencia: la potencia que se pierde en el puerto adaptado de salida y las diferentes condiciones de carga de los dispositivos activos. El amplificador distribuido *'power recycling'* se presenta como una alternativa a otras estructuras de potencia distribuidas ofreciendo condiciones de adaptación a la entrada ideales, idénticas condiciones de carga para todos los dispositivos activos, una combinación de potencia perfecta a la salida y un sistema de control de ganancia que está determinada por un acoplador direccional a la entrada. Gracias a las características previamente expuestas, esta nueva arquitectura podría ser de interés para aplicaciones de alta frecuencia donde la potencia de salida disponible de los dispositivos activos es escasa y la combinación de potencia es una necesidad. Además, el incremento de ganancia en ciertos rangos de frecuencia puede ser crucial para alcanzar los requisitos establecidos en aplicaciones potenciales.

La verificación experimental de las ideas expuestas en los capítulos anteriores se presenta en el ***Capítulo 4***. Por esta razón, dicho capítulo es clave en la presente Tesis doctoral. En el capítulo, se recopilan los resultados experimentales publicados en [16]. En dicha publicación se presentan las primeras medidas de un amplificador distribuido de potencia utilizando celdas CRLH diseñadas para trabajar en $\theta = 0$ a la frecuencia de operación, lo cual es prueba de la viabilidad del diseño de un amplificador distribuido de potencia basado en metamateriales. La teoría que se expone en [16] se ha utilizado, recientemente, por Fei y otros autores [41] para la implementación de un amplificador de potencia 2-D para la banda de 60 GHz en tecnología CMOS de 65 nm, lo cual demuestra que el concepto se puede extender a

otras tecnologías de fabricación. Las medidas en régimen de pequeña y gran señal que se han llevado a cabo en dicho primer prototipo han confirmado las conclusiones derivadas del análisis intrínseco simplificado. Los valores de ganancia son consistentes con la teoría, y la potencia de salida y la eficiencia demuestran que el amplificador está trabajando como un combinador óptimo en clase A. Una segunda versión de dicho prototipo se diseñó con el objetivo de verificar las conclusiones obtenidas en el capítulo 3. Para ello se diseñó un amplificador distribuido basado en líneas de transmisión CRLH en configuración *'power recycling'*. El prototipo se midió en régimen de pequeña señal para corroborar las conclusiones derivadas del anális teórico del PRDA. Las medidas evidencian el incremento de la ganancia predicha por la teorá junto con unas condiciones de adaptación a la entrada excelentes. Este mismo prototipo se ha comparado a las configuraciones *'single'*- y *'dual-fed'* confirmando la superioridad de los resultados del PRDA. Estos resultados muestran la viabilidad del amplificador de potencia distribuido como un combinador óptimo de potencia con el beneficio añadido de un incremento en la ganancia, que se puede seleccionar de forma arbitraria a través de un diseño apropiado del acoplador direccional, con unas condiciones de adaptación a la entrada casi perfectas. El capítulo concluye con un diseño de amplificador distribuido de potencia en tecnología monolítica. Este último diseño posee dos características interesantes: en primer lugar, supone el salto tecnologógico hasa la tecnología monolítica, lo cual es deseable para trabajar a frecuencias elevadas, y en segundo lugar, estudia el comporatmiento del amplificador distribuido de potencia bajo esquemas de modulación complejos. El amplificador que se ha diseñado, para aplicaciones de LTE, se ha simulado en condiciones de pequeña y gran señal, así como de señales moduladas, evidenciando buenos resultados en términos de ACPR y EVM.

Por último, el trabajo contenido en el ***Capítulo 5*** aparece como la continuación natural del análisis previamente desarrollado. El capítulo revisa los difrentes modos de operación de alta eficiencia y recupera el análisis que se llevó a cabo en el capítulo 2 para estudiar el comportamiento de los amplificadores distribuidos de potencia cuando se le aplican distintas estrategias al conformado de los armónicos. De dicho capítulo se extrae que es posible extrapolar el diseño de amplificador distribuido de potencia a cualquiera de los modos clásicos de alta eficiencia, tales como el A, B, AB ó C, y también la clase F inversa. Sin embargo, los modos que necesitan una carga

compleja en el fundamental, como por ejemplo la Clase E, no son implementables. Se han present ado simulations para respaldar los resultados teó ricos, y se presente un diseño de un amplificador distribuido de potencia en Clase AB en configuración *'power recycling'* utilizando un dispositivo HEMT de 8W de GaN sin encapsular. Los resultados muestran que es possible diseñar un amplificador distribuido de potencia trabajando como un combinador óptima de potency con altos niveles de eficiencia e incremento de ganancia.

Líneas futuras

Las líneas futuras de trabajo se enumeran a continuación:

1. Fabriación de un amplificador distribuido de potencia de alta eficiencia: esta tare es la continuación natural del trabajo presentado en el Capítulo 5. Al final de dicho capítulo, se presentó un diseño de un amplificador distribuido de potencia en Clase AB. Evidentemente, el siguiente paso consiste en la fabricación y medida del mismo con un esquema de modulación acorde con la frecuencia de trabajo, que pudiera beneficiarse del incremento en los valores de eficiencia de dicho diseño. Por supuesto, este tipo de diseños tienen sentido cuando se emplean dispositivos que cuentan con una alta densidad de potencia de salida, como por ejemplo un dispositivo de GaN. En este contexto, el trabajo descrito en la Sección 5.4, que se ha llevado a cabo con un dispositivo de Cree de 8W, encaja perfectamente con las futuras expectativas.

2. Inclusión de un mecanismo para el ajuste de fase en la arquitectura PRDA: puesto que las condiciones de fase son un requisito clave para conseguir el correcto funcionamiento de la arquitectura PRDA, es deseable incluir algún tipo de mecanismo que pudiera actuar como un ajuste fino en las condiciones finales de fase una vez que el prototipo esté construido. La idea es incluir un mecanismo de ajuste de fase controlado por tensión entre el acopolador direccional de entrada y el amplificador distribuido de 4 puertos, que pueda controlarse con un puerto externo.

3. Estudio analítico del comportamiento intrínseco de los amplificadores distribuidos de potencia no uniformes: en esta Tesis se ha llevado a cabo un

estudio extenso del comportamiento intrínsecto de los amplificadores distribuidos de potencia uniformes, y se han señalado las condiciones particulares que deben cumplir para conseguir combinación óptima de potencia a la salida. Sería interesante continuar dicho enfoque realizando un análisis de de los amplificadores distribuidos de potencia no uniformes. Se han publicado varios trabajos a lo largo de los años [10; 11; 19; 21] que han conseguido buenos resultados modificando las celdas unitarias entre etapas en la línea de drenador y la periferia de los dispositivos activos. El objetivo es conseguir expresiones generales que incluyan los casos particulares que ya se han publicado.

4. Escalado en frecuencia: la último tare que se propone está relacionada con las aplicaciones potenciales del PRDA. El elemento clave del PRDA reside en su mecanismo de control de ganancia que se puede conseguir a través de un diseñ adecuado del acollador direccional, a la vez que se consiguen condiciones de adaptación a la entrada casi perfectas. Esta característica podría tener interés a frecuencias elevadas, donde la potencia de salida es escasa y la ´unica manera de alcanzar los requisitos de los estándares de comunicaciones es a través de la combiandción de potencia. Tener un grado extra de libertad relacionado con la ganancia disponible puede marcar la diferencia entre una arquitectura y otra. Por lo tanto, es interesante y deseable escalar el diseño arriba en frecuencia para obtener todo el potencia de esta arquitectura innovadora. El concepto se ha validado recientemente por Fei y otros autores [41] para el rango de los 60 GHz con el diseño de un amplificador de potencia distribuido en 2-D con desfase cero en tecnología CMOS de 65nm que se basa en el trabajo [42], publicado el el autor de dicha Tesis. Por ello, hay buenas expectativas para el diseño en tecnología monolítica que se ha presentado en la Sección 4.3.

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